Optimized Design of a DCM Single-Input Dual-Output DC-DC PFM Boost Converter Featuring Zero Current Detection

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Optimized Design of a DCM Single-Input Dual-Output DC-DC PFM Boost Converter Featuring Zero Current Detection

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Abstract: *This study introduces the design of a Discontinuous Conduction Mode (DCM) Single-Input Dual-Output DC-DC Pulse Frequency Modulation (PFM) Boost Converter with Zero Current Detection (ZCD) aimed at addressing the diverse power supply needs of modern electronics. The converter, a synchronous boost type, efficiently produces two distinct output voltages (3.3 V and 5 V) from a single 1.8 V input, simplifying the control system requirements. Utilizing a 180 nm CMOS process for the control circuits, the design ensures seamless integration and efficient performance. Simulation results confirm the successful voltage amplification, achieving the target outputs of 3.3 V and 5 V. Additionally, the converter attains a peak efficiency of 82.93% across a load current range of 100µA to 1mA, making it ideal for a wide range of electronic applications. Key benefits of this design include its dual-output functionality, high efficiency, and compact integration, which collectively enhance the versatility and energy efficiency of power management solutions.*

Keywords: DC-DC Converter; Boost Converter; Single-Input Dual-Output; Zero Current Detection; Power Management

1. INTRODUCTION

The prevalence of battery-powered portable electronic devices, such as smartphones and tablets, has increased in recent years. As these devices often operate in standby or sleep mode, the power efficiency of the converters under light loads has become a crucial design consideration to prolong battery life [1]. DC/DC converters, including boost converters, are designed to handle an unregulated DC voltage from sources like PV arrays and maintain a controlled average DC output voltage. This is achieved by manipulating the durations of the energy absorption and injection intervals within each switching cycle [2,3]. DC-DC boost converters are widely used in portable electronics to step up the input voltage and provide the required output voltage levels. These converters offer advantages like high power density, efficiency, and reduced electromagnetic interference [4].

The boost converter operates in two distinct modes - Discontinuous Conduction Mode (DCM) and Continuous Conduction Mode (CCM) - depending on its energy storage capacity and the relative length of the switching period [5]. One effective approach to improve the efficiency of DC-DC boost converters is through Pulse Frequency Modulation (PFM) control. PFM minimizes switching losses by modulating the switching frequency based on the output voltage and current, making it particularly useful under light load conditions where traditional fixed-frequency control methods can lead to reduced efficiency [6].

PFM is a switching method commonly used in DC-DC voltage converters to improve efficiency at light loads. Unlike Pulse Width Modulation (PWM), which varies the width of square pulses at a constant frequency, PFM fixes the pulse width and varies the frequency. Therefore, it has advantages like better low-power conversion efficiency and reduced switching losses [7, 13-19].

The PFM control strategy relies heavily on the Zero Current Detector (ZCD), which detects the zero-crossing point of the inductor current. The ZCD triggers adjustments in the switching frequency, ensuring efficient operation in Discontinuous Conduction Mode (DCM) under light loads [8]. The ZCD is a critical component in PFM-controlled DC-DC boost converters, and its design and implementation are crucial for achieving high efficiency and low line and load regulation.

2. REVIEW OF RELATED LITERATURE

The work of Inguito et. al [9], shown in Table 1, provides insights into the application-specific design considerations and challenges related to WSNs, making it relevant to the thesis topic.

Sheu, M. L. et al. [10] present innovative design aspects related to dual-output converters, offering valuable insights into the design considerations for dual-output configurations and efficiency optimization. Chen, H. M. et al. [11] contribute to the field of boost converters with a focus on efficiency enhancement, aligning with this paper the emphasis on improving efficiency and incorporating zero current detection mechanisms in boost converters.

The related literature mentioned provides a comprehensive set of insights and design considerations related to boost converters, with a focus on dual-output configurations, efficiency enhancement, and practical implementation.

Table 1. Summary of Related Studies

Parameters	[9]	[10]	[11]	This work
Technology	180nm CMOS	180nm CMOS	180nm CMOS	180nm CMOS
Supply Voltage	1.8V	0.5V - 1.8V	1.2V	1.8V
Output Voltage	3.3V and 5V	1.8 and 3.3V	1.8V	3.3V and 5V
Load Current	20mA - 220mA	30mA	1mA- 50mA	1µA -1mA
Efficiency	83.4% at 220mA * at < 220mA	80.7% at 30mA	78.12% at 1mA	82.93% at 1mA
Mode	PWM	PFM	PFM	PFM
ZCD	No	No	Yes	Yes
Topology	Single Input – Dual Output	Single Input – Dual Output	Single Input – Single Output	Single Input – Dual Output
Synchronous	Yes	No	Yes	Yes
DCM or CCM	CCM	DCM	DCM	DCM

*Reference [9] does not specify the efficiency for currents below 220mA. However, it mentions that the efficiency ranges from 78% to 83.4% for load currents between 10mA and 220mA.

Table 1 compares various parameters and performance metrics of different studies related to power management ICs, highlighting the advantages of this work compared to others. All entries utilize 180nm CMOS technology, ensuring a fair comparison. This work operates at a supply voltage of 1.8V and offers dual output voltages of 3.3V and 5V, like Reference [9], but provides higher output voltage levels than the other references. It supports a wide load current range from 1µA to 1mA, significantly lower than the ranges in other studies, indicating superior efficiency and versatility for low-power applications. With an efficiency of 82.93% at 1mA, this work is competitive, particularly for low currents, a crucial advantage for energy-efficient designs. Operating in Pulse Frequency Modulation (PFM) mode, like References [10] and [11], it ensures low-power consumption at light loads. Additionally, it includes zero current detection (ZCD), which improves efficiency by reducing losses during zero current conditions. This is beneficial for low-power applications and is absent in Reference [9]. Employing a single input–dual output topology aligns with most of the references and provides flexibility for systems requiring multiple voltage levels. The synchronous operation, shared with References [9] and [11], enhances efficiency by reducing switching losses. Operating in Discontinuous Conduction Mode (DCM), like References [10] and [11], it further improves efficiency at light loads. Overall, this work demonstrates significant improvements and advantages, particularly in low-power applications, compared to the other references.

3. RESEARCH METHODS

This section explains the methodology of research and, at the same time, provides a comprehensive discussion. The discussion can be made in several sub-sections.

3.1 System Design Flow

This section addresses the first objective, which involved the steps in developing the whole system, starting from the design flow down to designing a DC-DC boost converter with a single input voltage and generating two output voltages.

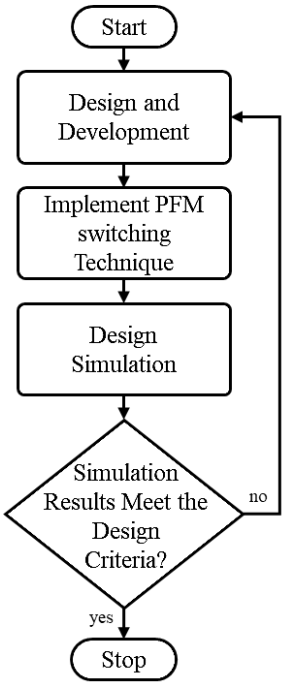

Fig. 1. System Design Flow

Figure 1 shows the Flowchart of the System Design, where it starts to the "Design and Development" stage. In this stage, the design process for the single input dual output DC-DC boost converter using the pulse frequency modulation (PFM) switching technique is initiated. The next step is to "Implement PFM Switching Techniques" in the design. This involves incorporating the PFM switching technique into the boost converter to achieve efficient operation at light loads.

Design Simulation is where simulations and analysis are performed to evaluate the performance of the boost converter. The flowchart then branches off to a decision point where the simulation results are evaluated to determine if they meet the design criteria. If the results meet the design criteria, the flowchart ends. If the results do not meet the design criteria, the flowchart loops back to the "Design and Development" stage.

3.1.1 System Design Block

The system diagram provides a visual representation of the single input dual output DC-DC boost converter. It illustrates the connections and interactions between the various components of the system, including the power stage, control circuitry, and input/output terminals.

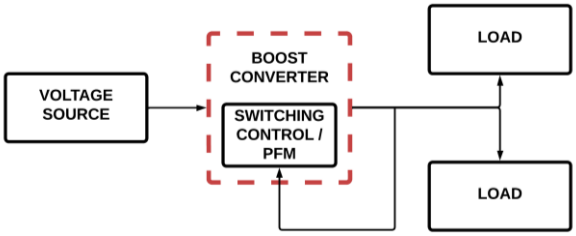

Fig. 2. System Design

To design a boost converter that steps up the 1.8 V input voltage to two output voltages, 3.3 V and 5 V, the pulse frequency modulation (PFM) technique is employed for switching control. The PFM technique allows for efficient and regulated voltage conversion by adjusting the switching frequency based on the load requirements. By implementing PFM, the boost converter can dynamically adjust the switching frequency to maintain stable output voltages at 3.3 V and 5 V while efficiently utilizing the input power.

3.2 Proposed Boost Circuit Schematic

Figure 3 shows the proposed design of the boost converter. This DC-DC boost converter is divided into two main stages: the power stage and the control stage. The control stage consists of several sub-circuits, including the voltage reference voltage, current sensor, hysteresis comparator, off-time controller, zero current detector, logic gates, and gate drive driver. The control stage is responsible for regulating the output voltage and ensuring stable operation of the converter. The power stage, on the other hand, is responsible for converting the input voltage to the desired output voltage.

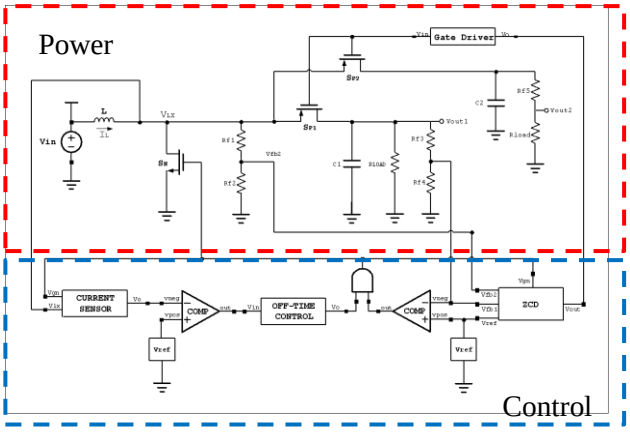

Fig. 3 Proposed Design of Boost Converter

3.3 Proposed Boost Circuit Schematic Design Flow

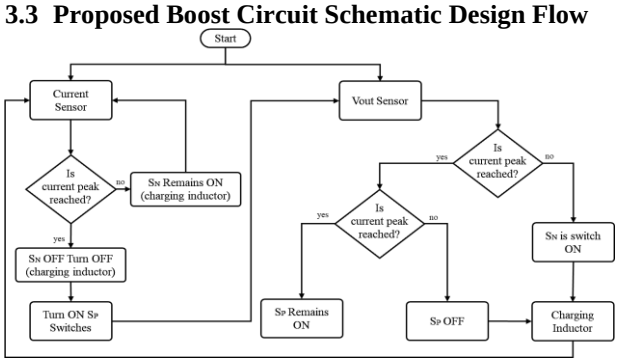

Fig 4. Proposed Design Flow

Figure 4 illustrates the system's operation. The process starts by measuring the inductor current and the output voltage (Vout) using the current sensor and Vout sensor (feedback). The current sensor monitors the inductor current. If the peak current is reached, it signals the system to stop charging (SN=0). Otherwise, charging continues. Once charging stops, switches on the load side (SP1 and SP2) activate, releasing the stored current. The Vout sensor constantly checks the output voltage. If it hasn't reached the desired level, the system restarts the charging cycle. When Vout reaches the target voltage, the system compares the voltage at the node Vlx with Vout to determine the appropriate on-time for the load side switches. If Vout drops below the desired level voltage, the system initiates another charging cycle, and the loop continues.

3.4 Design Specification

The proposed design of the DC-DC boost converter features a single input and a boosted dual output that utilizes Pulse Frequency Modulation (PFM) as the switching technique. The desired specifications of the boost converter are presented in Table 2.

Table 2. Design Specification

Parameters	Desired Values
Technology	180nm - CMOS
Input Voltage Range	1.8V
Voltage Output	3.3V and 5V
Efficiency Conversion	$\eta > 80\%$
Minimum Loading Current	100µA
Maximum Loading Current	1mA

The proposed design employs the 180nm CMOS Process technology, with an input voltage of 1.8 V and expected output voltages of 3.3V and 5V. The design ensures that the system can operate with a minimum loading current of 100µA and a maximum loading current of 1mA.

3.5 Current Sensor

The current sensor used in this study, as proposed in Tao, X., & Xu, J. (2008) [12], Figure 5 takes a different approach by eliminating the need for an error amplifier. This simplifies the design and offers several advantages. For instance, it reduces the overall cost by avoiding additional components. Additionally, it minimizes the die area required on the integrated circuit, leading to a more compact design. Furthermore, this design lowers power consumption. While some error amplifier implementations offer more power consumption, the sensing signal is not absolutely accurate.

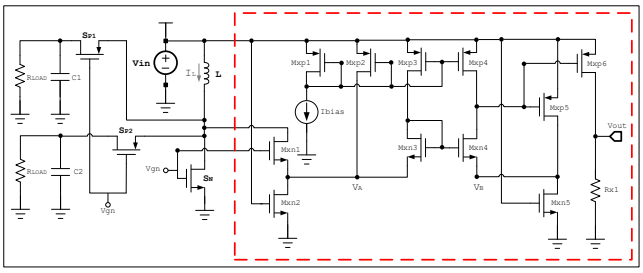

Fig. 5 Current Sensor Circuit

3.6 Off-Time Control

The off-time control circuit offers valuable functionality for enhancing the performance of the designed Current Sensor. This setup enables precise control over when the current sensor is active, allowing it to operate selectively during specific time intervals defined by the pulse signal. By utilizing the logic AND gate, the circuit ensures that the current sensor only senses current when the pulse generator or Vpulse signal is present, offering a controlled off-time mechanism.

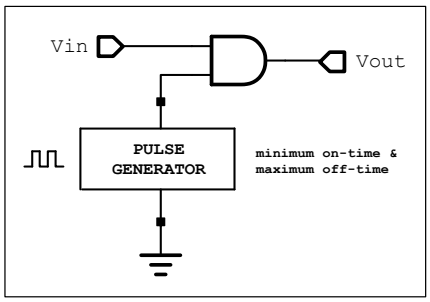

Fig. 6. Off-time Control Circuit

3.7 Bias Circuit

This circuit configuration can be effectively utilized as a voltage reference for the designed hysteresis comparator. The comparator can accurately compare input signals against this reliable reference voltage by leveraging the stable voltage levels established within this bias circuit. The precise and controlled voltage levels maintained by the bias circuit ensure that the comparator operates within the desired parameters, enhancing the accuracy and reliability of the comparison process. The structured connections within the bias circuit provide a solid foundation for the comparator to effectively assess input signals against a consistent and well-defined voltage reference, facilitating optimal performance and functionality in the overall circuit design.

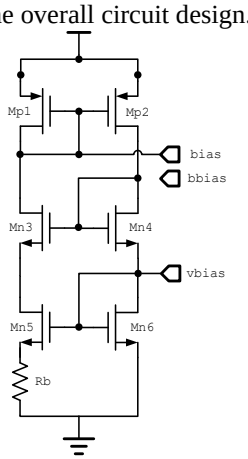

Fig.7 Bias Circuit

3.8 Driver

Within a feedback-controlled system, a gate driver circuit becomes essential to boost and refine signals traversing through multiple circuit blocks, compensating for losses, and optimizing the signal quality before reaching the final boost output, as depicted in Figure 8 showcasing a dual-stage inverter acting as the signal driver for the Power MOS switches.

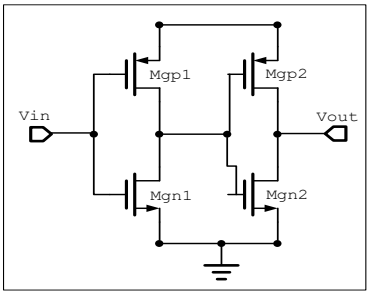

Fig. 8 Gate Driver

3.9 Power Stage

The power stage of the designed DC-DC boost converter consists of an inductor, capacitors, PMOS switches, and NMOS. PMOS was used on the high side of the switch, and NMOS on the low side. To maintain stable output voltages, a feedback loop was employed to regulate the switching frequency of the switch based on the voltage level of the two outputs. The power stage devices are connected, as shown in Figure 9.

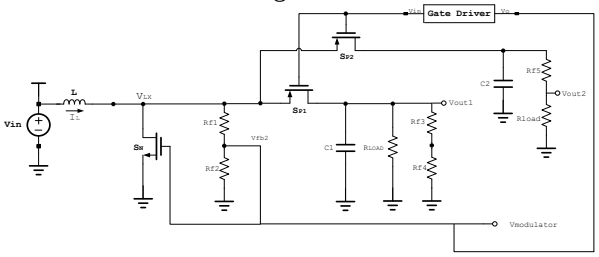

Fig. 9 Power Stage

3.10 Discontinuous Conduction Mode

To maximize efficiency, the converter's operation mode is set to discontinuous conduction mode (DCM). The type of operation was applied as it gives advantages, which are minimal switching losses at low load currents.

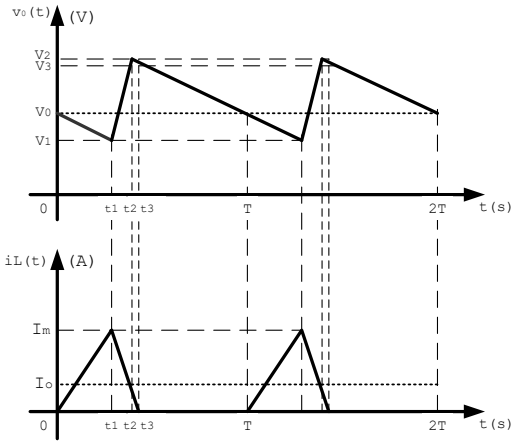

Fig. 10 Vo(t) and iL(t) of Discontinuous Conduction Mode Boost Converter (DCM)

As shown in Figure 10, the DCM boost converter operates by progressively increasing the inductor current during the switch's on-time. Once the current reaches its peak, the switch turns off. The inductor current then decays to zero and stays at zero during a period called the

off time before the cycle repeats with the switch turning on again.

3.11 Zero Current Detector

The design incorporates a zero-current detector (ZCD) to enhance the boost converter's power efficiency. This ZCD utilizes two hysteresis comparators comprised of transistors, Mzp1, Mzn1, and Mzn2, along with a set-reset latch. This configuration effectively eliminates reverse current through the high-side switch during the energy release phase. Additionally, the ZCD prevents both early and delayed detection of zero current, ensuring stable operation in discontinuous conduction mode (DCM).

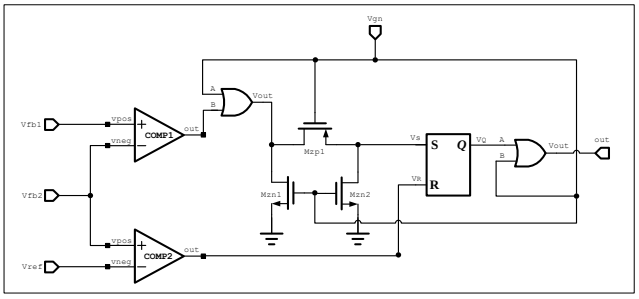

Fig. 11 Zero Current Detector

During the on-time, a high control voltage (VGN) activates the power switch (SN) and transistors (Mzn1 and Mnz2). This allows inductor current (IL) to flow and ramp up linearly until it reaches the peak current. The hysteresis comparator (COMP2) detects this peak and generates a high voltage (VR) that resets the control voltage (VQ) to low by the SR latch.

When VGN transitions from high to low (off-time), both inputs (VS and VR) to the SR latch become low, maintaining the low state of VQ. Consequently, the node Vout becomes low, turning on the power switch (SP). During this energy release phase, the stored energy in the inductor (L) is delivered to the output capacitor (Cout) and the load.

Also, the ZCD circuit ensures stable operation in discontinuous conduction mode (DCM). If the output voltage (Vout) exceeds the voltage at node Vlx, comparator COMP1 detects this difference. It then generates a high voltage through transistor Mzp1, the SR latch, and the SP gate driver, effectively turning off switch SP. This action eliminates reverse current through the switch, contributing to stable DCM operation.

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4. RESULTS AND DISCUSSIONS

This chapter presents the simulation results and discussions of the proposed system, providing insights into its performance, behavior, and potential areas for optimization.

4.1 Boost Converter

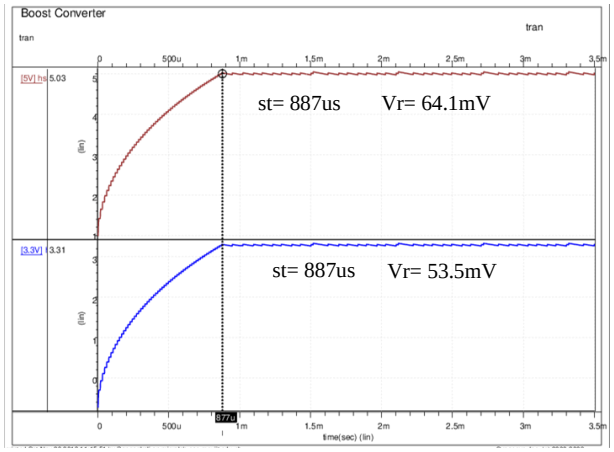

Fig 12. Simulation of the Design Boost Converter with Single Input-Dual Output

Figure 12 illustrates that the designed boost converter could produce two distinct amplified voltages, 3.3V and 5V, from an input of 1.8V. Both output voltages have a settling time of 887 µs. The output voltage ripples at 3.3V output and 5V output are 53.5mV and 64.1mV, respectively.

4.2 Line Regulation

Line regulation was performed to determine the ability of the converter to maintain a consistent output voltage even when the input voltage fluctuates. The test involves varying the input voltage within a specific range, in this case, ±10% of the input voltage (1.8V) and observing the output voltage.

As shown in Figure 13, the designed converter exhibits excellent line regulation, responding to input voltage changes and maintaining a stable output voltage. However, it's important to note that while the converter excels in line regulation, any input voltage variations will introduce ripple voltages that can directly affect the. output voltage quality.

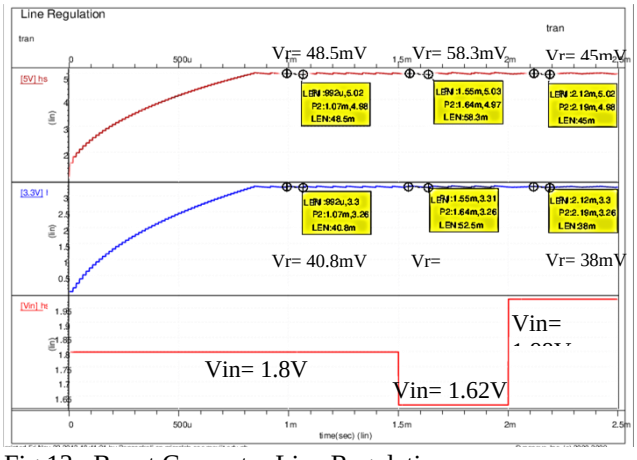

Fig.13. Boost Converter Line Regulation

4.3 Load Regulation

Load regulation is the ability of the system to maintain a stable output voltage despite variations in the output load current. The test involved simultaneously connecting the converter's output to varying loads, ranging from 100uA to 1mA, shown in Figure 14. The simulation results regarding output voltage ripple were inconclusive – no significant change in ripple amplitude was observed with varying load currents. However, an increase in ripple frequency was identified as the load current increased.

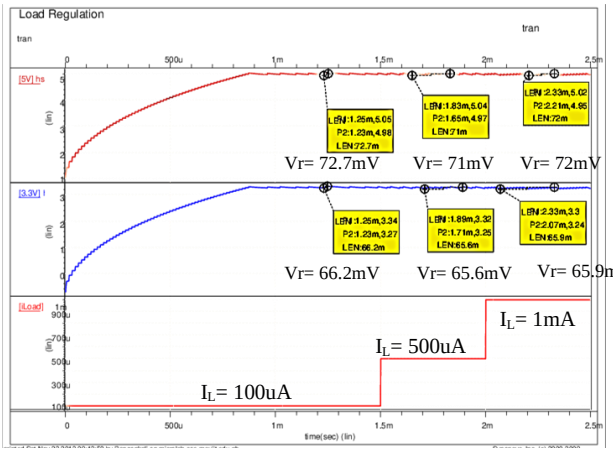

Fig.14. Boost Convert Load Regulation

4.4 System Limitation Test

To determine its system capabilities, it was tested with a range of load currents, from a minimum of 1 µA to a maximum of 1.5 mA.

As shown in Figure 15, the system can operate and deliver the desired output voltages even at the lowest load current,1 µA. However, as the load current increases beyond 1.1 mA, it starts to give an output voltage lower than the desired output voltage. This indicates that the system is suited only for very light load applications, with a maximum capacity of approximately 1.1 mA load current. While the system can still function at 1 µA, its power efficiency is significantly reduced, and it almost reaches zero. This statement was proved in Figure 16

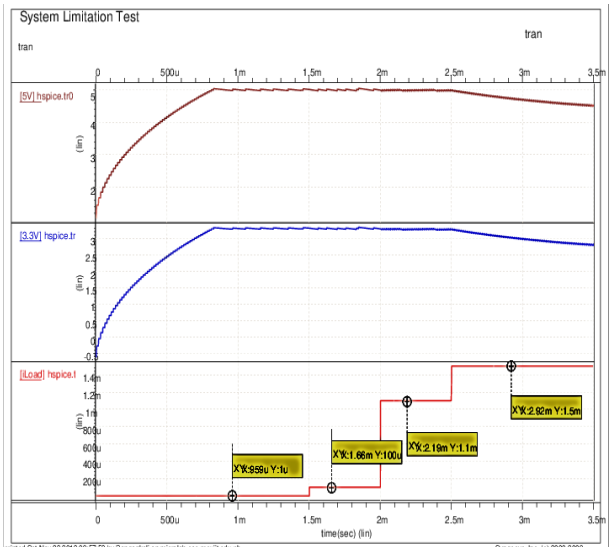

Fig.15. System Limitation Test

4.5 Power Efficiency

The power efficiency of the converter is determined by the ratio of its output power to its input power which can be directly measured using the 180nm CMOS technology. Figure 16 shows the line graph of the efficiency vs. the output load current.

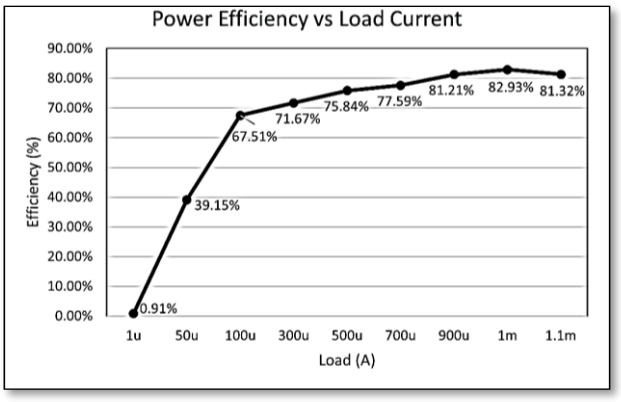

Fig 16. System Limitation Test

As shown in Figure 16, the boost converter design has a maximum efficiency of 82.93% at a 1mA load current. Although the efficiency decreases as the load current decreases, the boost converter still has decent power efficiency at 100uA load, which is the minimum current load parameter of system specification. This concludes that the system was able to function at very light load conditions.

5. CONCLUSION

This paper presents a successful implementation of a Single Input Dual Output DC-DC PFM Boost Converter with a Zero Current Detector. The boost converter successfully produces the 3.3 V and 5 V outputs. The design can achieve a maximum efficiency of 82.93% at 1mA load, which is a significant improvement over traditional Boost Converters. The paper discusses the importance of the Zero Current Detector and PFM in improving the efficiency of the converter. It concludes that the proposed design is a promising solution for improving the efficiency of boost converters and reducing power consumption in electronic devices.

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