

Study on defect characterization of Ge gate stacks using deep-level transient spectroscopy

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Study on defect characterization of Ge gate stacks using deep-level transient spectroscopy

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Abstract

Si ultra large scale integration (ULSI) industry has met the limitation on scaling. To keep improving the performance of metal-oxide-semiconductor field-effect transistors (MOSFETs), changing channel materials to high mobility materials is necessary. Ge is an attracting candidate due to its high electron and hole mobilities. A high-quality gate stack is the key to the high mobility Ge MOSFET, and a GeO₂ interlayer can reduce the interface traps (ITs); however, border traps (BTs) in GeO₂ and/or other oxide layers remain a problem. To reduce these traps and improve the quality of Ge gate stacks, a trap characterization of Ge gate stacks is necessary. Aim of this study is to develop a BT evaluation method and characterize the Ge gate stacks by using deep-level transient spectroscopy (DLTS) with a lock-in integrator. In this study, two kinds of Ge gate stacks are characterized, and the influence of BTs and ITs on Ge p-MOSFETs are studied.

The equations of IT density (D_{it}) and BT concentration (N_{bt}) in Ge metal-oxide-semiconductor capacitor (MOSCAP) were derived for a lock-in DLTS. Since IT and BT are applicable to different equations, signal identification and separation are important. The bias selecting for measurement was clearly defined. Due to the different capture and emission mechanisms of IT and BT, D_{it} and N_{bt} show different units.

IT and BT signals were successfully separated based on their different dependences on the intensity of injection pulses, and the BTs in GeO₂ were evaluated through investigating MOSCAPs with SiO₂/GeO₂/Ge gate stacks fabricated by thermal and plasma oxidation. By using p-type MOSCAPs, BTs at the position of 0.4 nm from GeO₂/Ge interface were measured. By using n-type MOSCAPs, BTs at the position range of 2.8–3.4 nm from the GeO₂/Ge interface were measured, of which N_{bt} varied little in the depth direction. The influences of the processing temperatures, oxidation methods, and Al-PMA on the quality of the gate stacks were clearly

observed. N_{bt} values of both p- and n-MOSCAPs are in the same range ($\sim 10^{18} \text{ cm}^{-3}$). Even though the N_{bt} value in n-MOSCAPs is not especially high, the low tunneling barrier allows the capture/emission process more aggressive. Passivation or elimination of BTs in GeO_2 near the conduction band edge of Ge is essential to realize high mobility Ge n-MOSFETs.

To investigate the BTs in other oxide materials, $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{p-Ge}$ gate stacks were characterized. Through evaluating the gate stacks with different GeO_x thicknesses, the respective BTs in Al_2O_3 , the $\text{Al}_2\text{O}_3/\text{GeO}_x$ interface region, and GeO_x were detected. D_{it} near the midgap is lower in the MOSCAPs with thicker GeO_x , while D_{it} near the valence band is lower in the MOSCAP with thinner GeO_x . The N_{bt} in Al_2O_3 ($6\text{-}9 \times 10^{17} \text{ cm}^{-3}$) is lower than those in GeO_x ($\sim 2 \times 10^{18} \text{ cm}^{-3}$), and the highest N_{bt} ($\sim 1 \times 10^{19} \text{ cm}^{-3}$) was found in the $\text{Al}_2\text{O}_3/\text{GeO}_x$ interface region.

To study the influence of ITs and BTs on mobility, Ge p-MOSFETs with $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{p-Ge}$ gate stacks were fabricated and analyzed. We confirmed that the ITs and the BTs near the valence band edge of Ge affect the mobility of Ge p-MOSFETs in the high-field region.

The BT evaluation method established in this study and the finding of the influence of ITs and BTs on mobility of p-Ge MOSFETs are an important step of the Ge MOSFETs improvement. The understanding may be also applicable to other materials or devices.

List of Abbreviations

AFM	Atomic force microscope
ALD	Atomic layer deposition
BLP	Bilayer passivation
BT	Border trap
CA	Contact annealing
CMOS	Complementary metal-oxide-semiconductor
C-V	Capacitance-voltage
DLTS	Deep-level transient spectroscopy
ECR	Electron cyclotron resonance
EOT	Equivalent oxide thickness
FET	Field-effect transistor
FLP	Fermi level pinning
HAADF	High-angle annular dark-field
IC	Integrated circuit
IT	Interface trap/state
<i>I-V</i>	Current-voltage
MOS	Metal-oxide-semiconductor
MOSCAP	Metal-oxide-semiconductor capacitor
PDA	Post-deposition annealing
PMA	Post-metallization annealing
PTO	Post-passivation thermal oxidation
PPO	Post plasma oxidation

rf	Radio-frequency
rms	Root mean square
RT	Room temperature
SRIM	Simulation result of the stopping and range of ions in matter
STEM	Scanning transmission electron microscopy
S/D	Source/drain
ULSI	Ultra large scale integration
VAP	Valence alternative pair
XPS	X-ray photoelectron spectroscopy

List of Symbols

Physics Constants

Quantity	Symbol	Values
Boltzmann constant	k	1.38×10^{-23} J/K 8.617×10^{-5} eV/K
Elementary Charge	q	1.602×10^{-19} C
Free electron mass	m_e	9.109×10^{-31} kg
Permittivity in vacuum	ϵ_0	8.854×10^{-14} F/cm
Planck constant	h	6.626×10^{-34} J s 4.135×10^{-15} eV s
Reduced Planck constant	$\hbar$	1.05×10^{-34} J s 6.58×10^{-16} eV s

Other Symbols

Symbol	Description	Units
ϵ_k	Dielectric constant of insulator (oxide)	no unit
ϵ_s	Dielectric constant of semiconductor	no unit
τ_c	Capture time constant of interface state/trap	s
τ_s	Emission time constant of trap in semiconductor	s
τ_{it}	Emission time constant of interface state	s

τ_t	Emission time constant of tunneling process	s
σ	Capture cross section	cm ²
$\sigma_{it,p}$	Hole capture cross section of interface state/trap	cm ²
σ_n	Electron capture cross section	cm ²
σ_p	Hole capture cross section	cm ²
Φ_{MS}	Work function difference between metal and semiconductor	eV
Ψ_B	Energy difference between the Fermi-level and intrinsic Fermi-level	eV
ϕ_s	Surface potential	eV
μ	Channel mobility	cm ² /Vs
C_{ox}	Oxide capacitance	F, F/cm ²
C_{dep}	Depletion region capacitance	F, F/cm ²
d	Insulator thickness	cm, nm
D_{it}	Interface trap/state density	eV ⁻¹ cm ⁻²
$\mathcal{E}_{GeO_2}$	Electric field strength in GeO ₂	MV/cm
$\mathcal{E}_{AP}$	Applied pulse intensity/electric field strength	MV/cm
E	Energy level	eV
E_c	Conduction band energy level	eV
$\mathcal{E}_{eff}$	Effective electric field	MV/cm
E_F	Fermi level	eV
E_{F_1}	Fermi level for holes at the interface at the end of the capture process	eV

E_{F_2}	Fermi level for holes at the interface in the emission process	eV
E_g	Band gap	eV
E_i	Intrinsic Fermi level	eV
$e_{it,p}$	hole emission rate from interface state	s ⁻¹
e_s	hole emission rate from trap in semiconductor	s ⁻¹
E_T	Energy level of bulk trap	eV
E_t	Tunneling barrier height	eV
e_t	hole emission rate of tunneling process	s ⁻¹
E_{tn}	Tunneling barrier height for n-MOSCAP	eV
E_{tp}	Tunneling barrier height for p-MOSCAP	eV
E_v	Valence band energy level	eV
f	Frequency	Hz
g_m	Transconductance	S
I_D	Drain current	A, A/μm
I_{DLTS}	DLTS signal intensity	1/pF ²
I_S	Source current	A, A/μm
J	Current density	A/cm ²
L	Channel length	μm
m_i^*	Insulator effective mass	kg
m_p^*	Semiconductor effective hole mass	kg

N_A	(Shallow) acceptor concentration	cm^{-3}
N_{bt}	Border/slow trap concentration	cm^{-3}
N_c	Effective density of states in conduction band	cm^{-3}
N_D	(Shallow) donor density	cm^{-3}
N_T	Bulk trap density	cm^{-3}
N_v	Effective density of states of valence band	cm^{-3}
$Q_{fix,eff}$	Fixed charge density	cm^{-2}
T	Temperature	K, °C
t	Time	s
T_p	Pulse period	s
t_w	Filling pulse duration	s
V_{AP}	Applied voltage above flatband voltage	V
V_D	Drain voltage	V
V_{FB}	Flatband voltage	V
V_G	Gate voltage	V
V_{TH}	Threshold voltage	V
$v_{th,n}$	Thermal velocity of electrons	cm/s
$v_{th,p}$	Thermal velocity of holes	cm/s
W	Channel width	μm

W_d	Depletion width	cm
z	Tunneling depth	cm
z_0	Depth measured by Lock-in DLTS under a certain frequency	cm

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Chapter 1 Introduction

1.1 Research background

Nowadays, there are more and more electronics containing ultra large scale integration (ULSI) circuits, which are mainly composed of Si devices, in our daily life, allowing convenient and diverse lifestyles. The production number of electronics is increasing, and so are the ULSI circuits inside. According to a forecast of electronic system semiconductor content shown in Fig. 1.1, which was calculated from the ratio of semiconductor market to electronic systems market in each year, the semiconductor content will keep raising in the coming years [1]. To improve the performance of ULSI, scaling technology has been applied, and post-scaling technology is being developed.

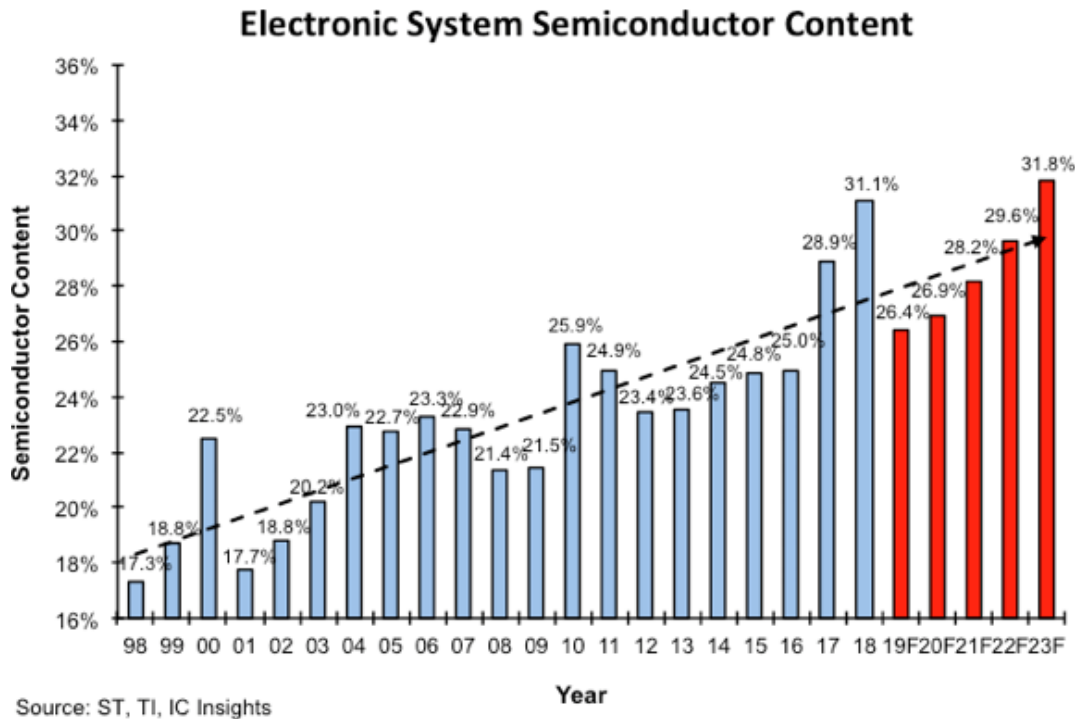


FIG. 1.1 Forecast of electronic system semiconductor content [1].

1.1.1 Scaling technology

The invention of monolithic integrated circuit (IC) chips can be dated back to 1957, when surface passivation process was developed and a concept of pn junction isolation was conceived, allowing transistors work independently on one chip [2]. Most of modern IC chips are metal-oxide-semiconductor (MOS) chips, containing MOS field-effect transistors (FETs), especially complementary MOS (CMOS) which consists of an n-MOSFET and a p-MOSFET.

MOSFET has components of a source, a drain and an insulator-gate, and carriers flowing from source to drain can be controlled by switching the gate voltage. The saturation drain current (I_D) is given by the following equation:

$$I_D = \frac{W}{2L} \mu C_{ox} (V_G - V_{TH})^2, \quad (1.1)$$

where W is the channel width, L is the channel length, μ is the channel mobility, C_{ox} is the gate capacitance, V_G is the gate voltage, and V_{TH} is the threshold voltage [3]. C_{ox} is given by

$$C_{ox} = \frac{\epsilon_0 \epsilon_k}{d}, \quad (1.2)$$

where ϵ_0 is the vacuum permittivity, ϵ_k is the dielectric constant of insulator (oxide), and d is the thickness of insulator. With the size of MOSFET shrinking, so-called scaling, not only the integration degree increases but also the power consumption decreases while the performance is kept [4].

The image of MOSFET scaling and the effects of scaling are shown in Fig. 1.2 and Table 1.1, respectively. Therefore, the power consumption was suppressed by scaling until the channel length is less than 100 nm. When the dimensions are on the nanoscale, short channel effect and gate leakage current become severe. Besides, the solubility limit of dopant leads to an increase in the parasitic resistance in source and drain. To solve these problems, post scaling technology was

developed.

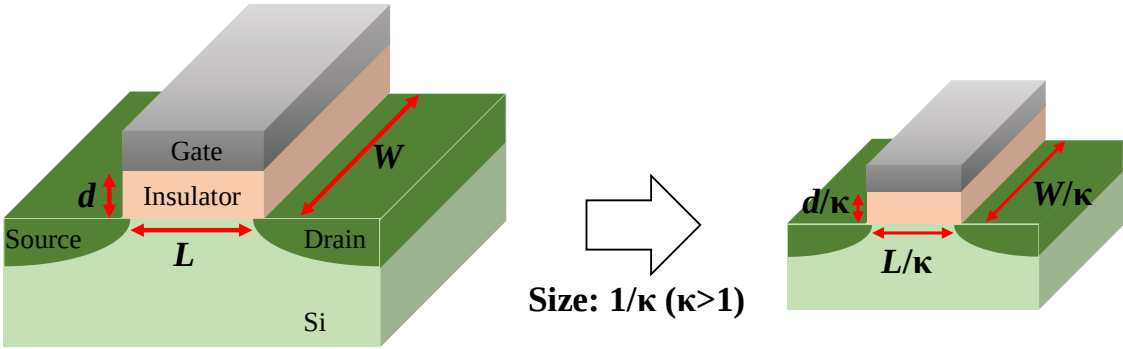


FIG. 1.2 An image of MOSFET scaling.

TABLE 1.1 Influence of scaling on performance of MOSFET.

Parameter	Scaling factor
Dimension L, W, d	$1/\kappa$
Doping concentration	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance C ($\epsilon A/d$)	$1/\kappa$
Integration degree	κ^2
Delay time t (CV/I)	$1/\kappa$
Power consumption P (IV)	$1/\kappa^2$

1.1.2 Post scaling technology

Post scaling technology is mainly focused on the gate stack and the channel mobility enhancement. According to Eq. (1.2), large C_{ox} can be achieved by not only decreasing d , but also increasing ϵ_k . Therefore, the commercial poly-Si/SiO₂ gate stack was replaced by metal/high- k gate stack, which has been commercialized in 2007 [5].

TABLE 1.2 Carrier mobilities and bandgap for Si, Ge and typical III-V compound semiconductors [10].

	Si	Ge	InP	GaAs	InAs	InSb
Electron mobility (cm ² /V s)	1600	3900	5400	9200	40000	77000
Hole mobility (cm ² /V s)	430	1900	200	400	500	850
Bandgap(eV)	1.12	0.66	1.34	1.42	0.36	0.14

To enhance the channel mobility or the drive current, some structural techniques, such as strained Si channel [6] and FinFETs [7], were studied and commercialized. However, these FETs will finally meet the physical limit on scaling. To keep improving the performance of MOSFET, high-mobility materials are considered as an appropriate way to realize high speed and/or low power consumption. Several materials have a higher mobility than Si, as shown in Table 2 [8]. Ge has the highest hole mobility among these materials, and its electron mobility is much higher than Si. Besides, Ge is the only elemental semiconductor, which has an advantage while compound semiconductor is stoichiometry-sensitive. The balanced electron and hole mobilities raise the potential of Ge CMOS. Although some groups suggested using Ge p-MOSFET combined with III-V compound n-MOSFET [8], it will be more difficult to apply to the current

Si ULSI [9,10]. Focusing on one substrate would be achievable in the current stage, and Ge seems a feasible candidate [11].

1.2 Issues of Ge MOSFETs

Although Ge has a high electron mobility and the highest hole mobility among the semiconductor materials, many problems still need to be solved. Based on the components of MOSFET, the problems can be categorized into metal/Ge ohmic contact, high-doping source/drain (S/D) and Ge gate stacks.

1.2.1 Metal/Ge ohmic contact

Forming an ohmic contact of metal and semiconductor is easy for p-type Ge but not for n-type Ge due to Fermi level pinning (FLP). FLP happening at the metal/Ge interface is a phenomenon that Fermi level of Ge is pinned at charge neutrality level near the valence band [12,13]. Since FLP was not observed at metal/oxide and oxide/Ge, inserting a thin oxide layer as a tunneling barrier between metal and Ge unpins the Fermi level at metal/Ge surface [14]. However, to alleviate the FLP, this oxide interlayer has to be over 1 nm, which raises the contact resistance. Another method without oxide insertion was reported [15]. Both ohmic contact for n-Ge and Schottky contact for p-Ge were achieved by TiN sputtering deposition followed by an annealing. The key to the FLP alleviation here is a nitrogen-contained amorphous interlayer, leading to electron density tuning and allowing a low resistance of metal/n-Ge contact.

1.2.2 High-doping S/D

For a MOSFET, doping is necessary for substrate ($10^{16}\sim 10^{18} \text{ cm}^{-3}$) and S/D ($>10^{20} \text{ cm}^{-3}$). In Si era, the conventional way of S/D doping is ion implantation followed by an annealing ($>700^\circ\text{C}$)

to activate dopants and recover the ion implantation damage. However, since the low melting point and instability of Ge, high temperature annealing is not suitable for Ge. B and Ga are promising dopants for p⁺ Ge due to the low diffusivity and high electrical activation [16]. By contrast, P and As are difficult to activate, and Sb is too large and heavy, which can cause serious deformation on substrate during ion implantation [17,18]. Therefore, instead of ion implantation, other methods, such as gas-phase doping [19], spin-on dopant [20] and in-situ doping [21], are recommended. In addition, compared to the rapid thermal annealing, laser annealing shows better activation [22,23].

1.2.3 Ge gate stacks

In the Si era, high quality of SiO₂/Si gate stacks was a key of a high-performance Si MOSFET. Even high-*k* materials are employed, a SiO₂ interlayer is the solution to the high-quality interface. Although it has been confirmed that a thermally grown GeO₂/Ge shows a high interfacial quality, GeO₂ is not as stable as SiO₂. GeO₂ decompose to gas-phase GeO and desorb at temperatures over 420 °C, and this can cause degradation of electrical properties [24–26]. Moreover, the hygroscopic property of GeO₂ is another concern that not only GeO₂ cannot survive from the cleaning process in fabrication, but also the reliability for air exposure is doubtful [27,28]. Therefore, growing GeO₂ interlayer without air exposure and stabilizing GeO₂ interlayer without degrading the interfacial property are the key to form a high-quality Ge gate stacks. Previously, our group developed a bilayer passivation (BLP) method, which enable the SiO₂/GeO₂/Ge structure without air exposure to GeO₂ [29]. Besides, an Al post-metallization annealing (PMA) is effective for improvement of interfacial quality, thus enhancing mobility of Ge p-MOSFET [30]. One other group also reported post plasma oxidation for Al₂O₃/GeO_x/Ge formation [31,32]. Both methods showed good interfacial qualities.

1.3 Characterization of Ge gate stacks

The high-quality gate stack is indispensable to high mobility Ge MOSFETs. One of the undesired defects in the gate stacks is interface trap/state (IT), which exist at the interface due to the interruption of a periodic lattice structure [33,34]. These ITs capture carriers with different time constant depending on their energy level and act as Coulomb scattering centers, thus degrading channel mobility. The other electrically active defect is in the oxide layers. They are usually called slow trap or border trap (BT) because the capture process is much slower and those close to the interface are more influential. The origin of BT is not clear yet and should be related to the materials and fabrication process of oxide layers. Since these traps can lead to channel mobility degradation, characterization and reduction of density of ITs (D_{it}) and of concentration of BTs (N_{bt}) are essential. ITs and BTs in a MOSFET are shown in Fig. 1.3.

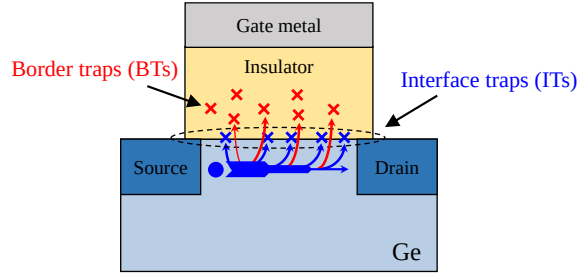


FIG. 1.3 Illustration of ITs and BTs capturing carrier and degrading channel mobility of a MOSFET.

1.3.1 D_{it} characterization

There are several methods for the D_{it} characterization, and some of them have been studied on Ge metal-oxide-semiconductor capacitors (MOSCAPs), such as high frequency capacitance voltage (C-V) [35], and conductance [36]. Both methods suggest low measuring temperature to avoid the influence of minority carrier generation and achieve high-accuracy measurements. In

Si era, deep-level transient spectroscopy (DLTS) was also used for D_{it} characterization [37–39], and the high-sensitivity DLTS enables determination of the D_{it} at mid $10^9 \text{ cm}^{-2}\text{eV}^{-1}$ range [40].

In DLTS measurement, a sufficient injection-pulse strength is commonly necessary to completely fill the ITs. However, DLTS signals were dependent on the injection-pulse strength, as shown in Fig. 1.4 [41], and the extracted D_{it} value ($4 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$) for a $\text{SiO}_2/\text{GeO}_2/\text{Ge}$ structure fabricated by BLP method, are higher than those ($5 \times 10^{10} - 1 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$) for GeO_2/Ge measured by other methods [42–44]. This implies that the DLTS results contain signals from oxide layer, thus overestimating the real D_{it} . Therefore, to obtain the accurate D_{it} , careful selection of the injection-pulse strength is important, and conventional DLTS measurement with constant bias throughout all temperatures is not suitable.

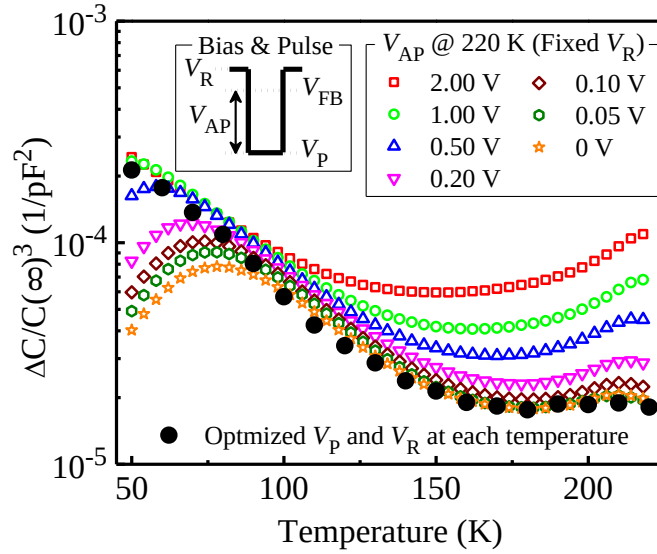


FIG. 1.4 DLTS signals of Ge p-MOSCAP. Open symbol: conventional DLTS measurement with constant pulse bias and reverse bias [41].

1.3.2 N_{bt} characterization

Some researchers have proposed a few methods based on the hysteresis of a C - V sweep

[45,46] or a time response of capacitance [47], and they all pointed out the high density of BTs in GeO₂/Ge n-MOSCAPs. However, the hysteresis of a C - V sweep depends on the scan speed and voltage range, and the method of the time response of capacitance is extremely time consuming, which therefore requires a high temporal-stability of the capacitance meter and a good durability of the MOSCAPs. Moreover, these two methods cannot provide the volumetric density of BT.

Actually, BTs also exist in the SiO₂/Si structure, and DLTS has been applied to N_{bt} evaluation for Si MOSCAPs [48,49]. However, owing to the relatively low N_{bt} in SiO₂ and the large band-offsets at the SiO₂/Si interface, BTs do not cause serious problems in Si MOSFETs. Therefore, N_{bt} evaluation by DLTS has not been intensely studied. As for the GeO₂/Ge structure, the BT problem becomes serious because the N_{bt} in GeO₂ is relatively high and the band offsets at the GeO₂/Ge interface are apparently lower than those of SiO₂/Si. As a result, if a DLTS measurement is performed for GeO₂/Ge MOSCAPs, the DLTS signal would be greatly contributed by BTs. In a previous study, when a GeO₂/Ge structure was measured, the DLTS signal intensity clearly increased with increasing intensity of the injection pulse (Fig. 1.4) [41], which must have resulted from the BTs in GeO₂. Because the BT signal can be clearly observed by DLTS, DLTS can be a promising method to evaluate BTs for Ge MOSCAPs. To our knowledge, N_{bt} evaluation of Ge MOSCAPs using DLTS has not yet been studied.

1.4 Aim and overview of the thesis

The aim of this study is to characterize the defects in Ge gate stacks using DLTS. In this study, two kinds of gate stacks were characterized, and Ge MOSFETs were fabricated and evaluated to study the influence of IT and BT on channel mobility. The BT characterization method established in this study will play an important role for improvement of MOS devices. Each of study is briefly described as follows:

1. DLTS analysis for D_{it} and N_{bt} in Ge MOSCAP

The principle of DLTS was studied, and equations of D_{it} and N_{bt} for Ge MOSCAP were derived for a lock-in DLTS. Since IT and BT are applicable to different equations, the importance of signal identification and separation is pointed out. The bias selecting for measurement was clearly defined. Due to the different capture and emission mechanisms of IT and BT, the D_{it} and N_{bt} shows different units.

2. DLTS study on $\text{SiO}_2/\text{GeO}_2/\text{Ge}$ gate stacks fabricated by thermal oxidation and plasma oxidation

DLTS signals were decomposed into IT signals and BT signals according to their features. D_{it} and N_{bt} of several MOSCAPs fabricated by thermal oxidation and plasma oxidation were investigated. BTs at the position of 0.4 nm from the GeO_2/Ge interface were measured for p-MOSCAPs. In the case of n-MOSCAPs, BTs at the position range of 2.8 to 3.4 nm from the GeO_2/Ge interface were measured. N_{bt} values of both p- and n-MOSCAPs are in the same range. The influences of the processing temperatures, oxidation methods, and Al-PMA on the quality of the gate stacks were also discussed. Even though the N_{bt} value in n-MOSCAPs is not especially high, the low tunneling barrier allows the capture/emission process more aggressive. Therefore, we suggested that passivation or elimination of states in GeO_2 with energy level near to conduction band edge of Ge are essential to realize high channel-mobility for n-MOSFETs.

3. DLTS study on $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{p-Ge}$ gate stacks fabricated by post plasma oxidation

For better understanding and performance improvement, BT in high- k gate stacks are a great interest. We characterized D_{it} and N_{bt} of $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{p-Ge}$ gate stacks with different

GeO_x thickness fabricated by PPO. By changing the thickness of GeO_x, N_{bt} in the GeO_x interlayer, the Al₂O₃/GeO_x interface region, and the Al₂O₃ layer, respectively, were measured. The D_{it} near the midgap is lower in the MOSCAPs with thicker GeO_x layer. By contrast, the D_{it} near the valence band is lower in the MOSCAPs with thinner GeO_x layer, owing to the defect termination by Al oxide. BTs are mainly located at the Al₂O₃/GeO_x interface region.

4. Study on influence of D_{it} and N_{bt} on performance of Ge p-MOSFETs with Al₂O₃/GeO_x/Ge gate stacks

Ge MOSFETs were fabricated to study the influence of IT and BT on channel mobility. It is confirmed that ITs and BTs near the valence band edge of Ge affect the effective mobility of Ge p-MOSFETs in the high-field region. Therefore, reduction of ITs and BTs near the valence band is the key to reach high-performance p-MOSFETs. We proposed that Al₂O₃ is a suitable dielectric material for Ge p-MOSFETs.

In chapter 2, the principle of DLTS and the basic measurement are introduced. Calculation of D_{it} and N_{bt} in GeO₂/Ge structure using DLTS are also presented. Chapter 3 contains characterization of IT and BT in SiO₂/GeO₂/Ge gate stacks fabricated by thermal oxidation and plasma oxidation. Separation of IT and BT signals is described. In chapter 4, we evaluated IT and BT in Al₂O₃/GeO_x/p-Ge gate stacks fabricated by post plasma oxidation were evaluated by using DLTS. The effect of BTs on the mobility of MOSFETs are also discussed. Chapter 5 presents the conclusions and the outlook.

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Chapter 2 Establishment of BT evaluation using DLTS

[1–3]

2.1 Introduction

DLTS is an instrument for investigation of electrically active defects, which can trap carriers in semiconductors. By changing the biases, carriers are captured and emitted from traps, and these attribute to a capacitance transient. A conventional DLTS is usually equipped with a boxcar integrator or a lock-in integrator to analyze the transient. Since lock-in DLTS provides a better signal/noise ratio, it is more common. According to the nature of defects, trap density and even trap type can be estimated. Even though the main principle for trap density extraction is the same, the details of the measurement and the calculation depend on devices and nature of defects. DLTS was firstly designed to characterize point defects in semiconductors through measuring Schottky diodes or pn junctions. Nowadays, some research groups are trying to evaluate extended defects in epitaxially-grown semiconductor films and interface state in MOS devices [4]. In this chapter, calculations of different types of traps will be introduced. All the equations refer to p-type substrate, and some details are specific for lock-in DLTS.

2.2 DLTS on Schottky diodes

As mentioned previously, DLTS was firstly used for characterization of point defects in semiconductor bulk, and Schottky diodes or pn junctions were common devices for DLTS measurement. Figure 2.1 shows the principle of DLTS on Schottky diodes. When a pulse bias is applied, bulk traps above Fermi level (E_F) capture holes. Some bulk traps become under E_F right

after the voltage changes to a reverse bias (V_R), thus emitting holes. After a certain time, all the bulk traps under E_F become empty. As a result, the capacitance transient $C(t)$ can be observed, as shown in Fig. 2.1(c). By analyzing the capacitance transient, bulk trap density (N_T) can be extracted with an approximation of $N_T \ll N_D$, which is given by

$$N_T = 2N_A \frac{|\Delta C|}{C(\infty)}, \quad (2.1)$$

where N_A is the shallow acceptor density, and $\Delta C = C(t) - C(\infty)$. Some details of the DLTS signals are discussed in Appendix.

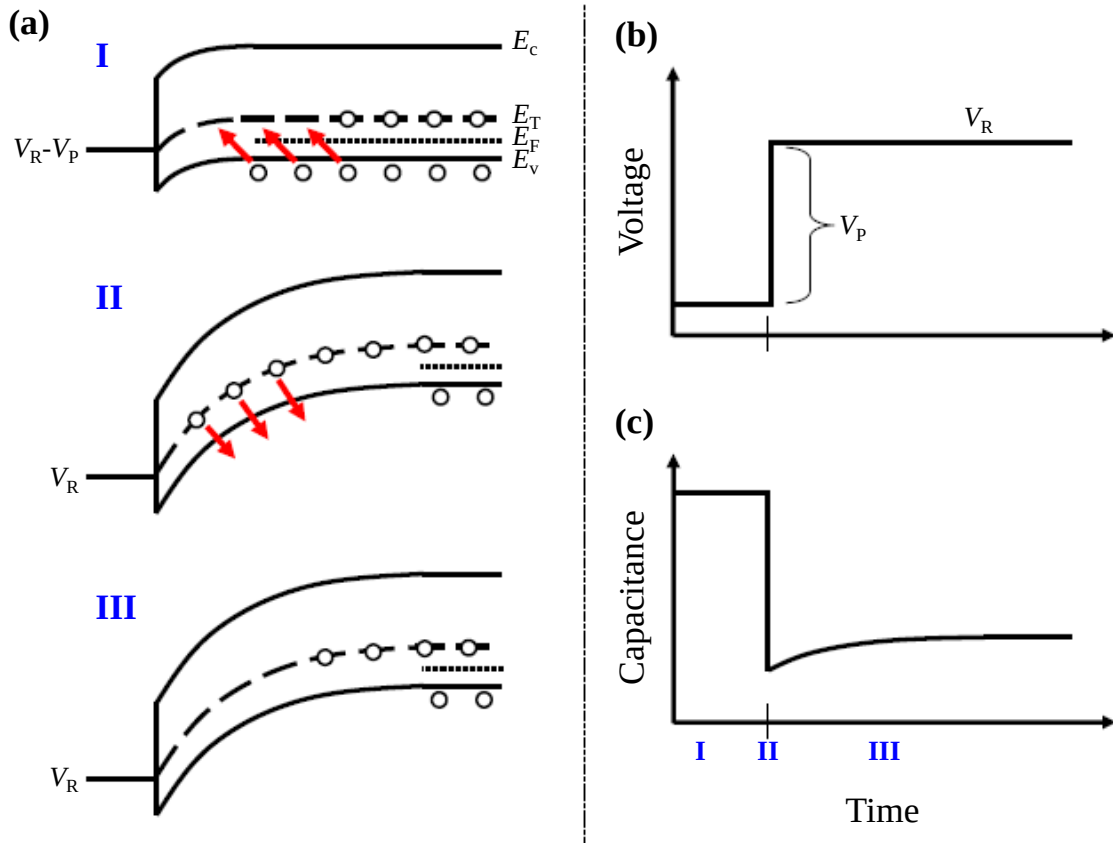


FIG. 2.1 Schematic of the contribution of bulk traps to the DLTS signals. (a) Band diagrams of a Schottky diode at different biases, (b) applied voltage and (c) capacitance.

Carrier emission from these traps is a thermally activated process. Therefore, emission time constant τ_s and emission rate e_s are given by

$$\tau_s = \frac{1}{e_s} = \frac{\exp\left(\frac{E_T - E_v}{kT}\right)}{\sigma_p v_{th,p} N_v}, \quad (2.2)$$

where E_T is the energy level of bulk trap, E_v is the valence band edge, k is the Boltzmann constant, T is the temperature, σ_p is the capture cross section of bulk trap, $v_{th,p}$ is the thermal velocity of holes, and N_v is the effective density of states in the valence band. According to Maxwell-Boltzmann distribution, $v_{th,p}$ is defined as

$$v_{th,p} = \sqrt{\frac{3kT}{m_p^*}}, \quad (2.3)$$

where m_p^* is the semiconductor effective hole mass. N_v is given by

$$N_v = 2 \left(\frac{2\pi m_p^* kT}{h^2} \right)^{\frac{3}{2}}, \quad (2.4)$$

where h is the Planck constant. If we define the constant terms in a product of Eq. (2.3) and Eq. (2.4) as one coefficient γ_p , which means

$$\gamma_p = \frac{v_{th,p} N_v}{T^2}, \quad (2.5)$$

then Eq. (2.2) can be rewritten as

$$\tau_s T^2 = \frac{T^2}{e_s} = \frac{\exp\left(\frac{E_T - E_v}{kT}\right)}{\gamma_p \sigma_p} \quad (2.6)$$

and

$$\ln(e_s/T^2) = \ln(\gamma_p \sigma_p) - \frac{E_T - E_v}{kT}. \quad (2.7)$$

The logarithmic form is so-called Arrhenius plot ($e_s/T^2 - 1/kT$). By fitting the plot with a straight

line, E_T and σ_p can be obtained from the slope and the intercept of the fitting line, respectively. Besides, by changing the filling pulse duration and observing the behavior of the peak intensity tendency, trap type, such as point defects and extended defects, which extend in one or more dimensions, can be distinguished. Figure 2.2 shows an example of different behaviors between point defects and extended defects [5]. The data are ΔC at peak position with the different filling pulse duration. Point defects exhibit exponential filling with pulse duration and saturate soon after a sudden raise. In contrast, extended defects, which could be dislocations, stacking faults, precipitates, etc., show a logarithmic filling behavior.

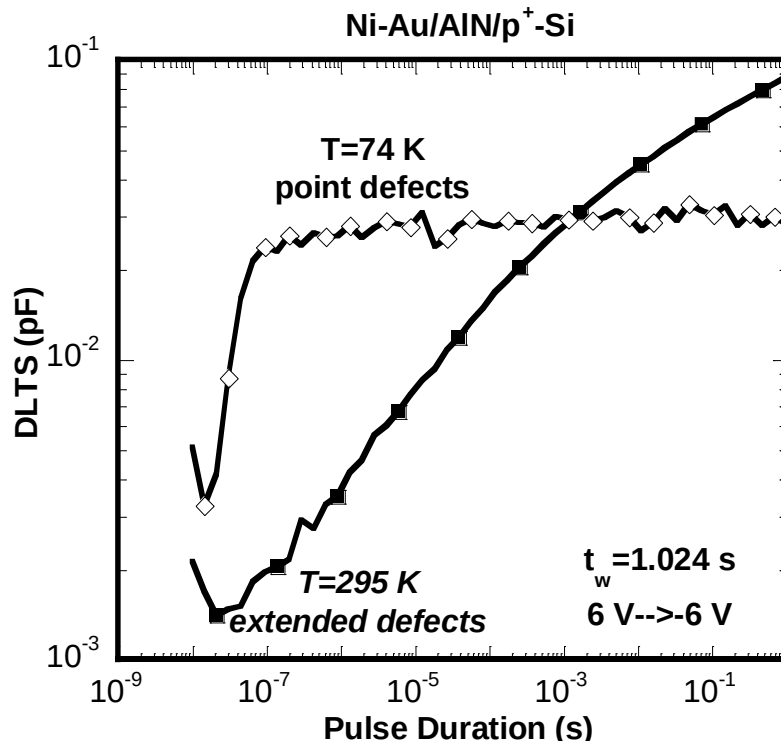


FIG. 2.2 Pulse filling behaviors of point defects and extended defects [5].

2.3 DLTS on MOSCAPs

In this section, most of equations are applicable to all general MOSCAPs, while some values are specific calculated for GeO_2/Ge structure. Owing to the features of capture and emission of carriers, the amount of ITs and BTs can be calculated by applying voltage pulse trains (for capture) and analyzing the capacitance during the emission process. Figure 2.3 shows the principle of DLTS on MOSCAPs. The experimental setup is shown in Fig. 2.3(a). In the case of a p-type MOSCAP, when a negative voltage pulse train is applied (Fig. 2.3(b)), a transient capacitance can be measured during the time between two neighboring pulses (Fig. 2.3(c)).

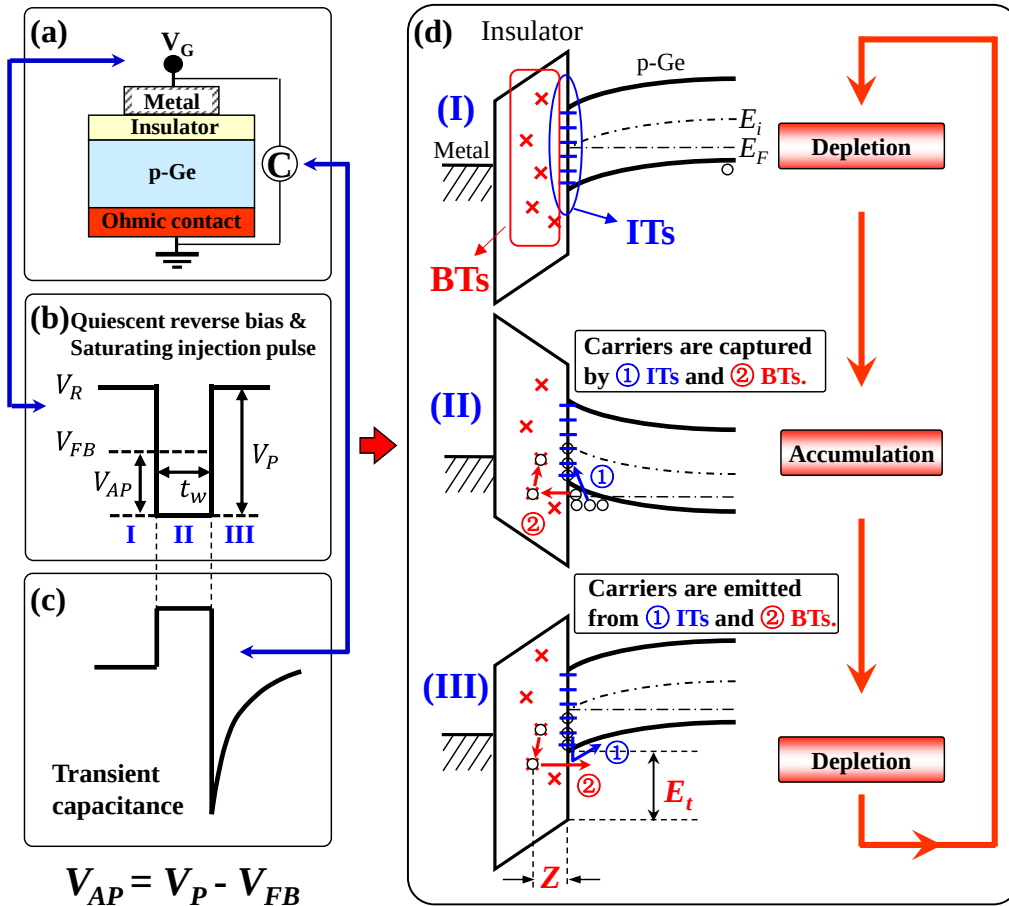


FIG. 2.3 Schematic of the contributions of ITs and BTs to the DLTS signals. (a) An experimental setup, (b) voltage transition, (c) capacitance transition and (d) band bending processes.

The band bending under different voltages is shown in Fig. 2.3(d). In region I, V_R causes depletion, and there is no hole (majority carrier) in the region near to the Ge/insulator interface. In region II, the voltage is lower than the flat-band voltage, thus causing accumulation. The holes accumulated near the interface have a chance to be trapped by the BTs and ITs located above E_F . However, the capture process for BTs is much slower than that for ITs, owing to the different capture mechanisms. In region III, V_R causes depletion again, and the holes are emitted from BTs and ITs located below E_F . This emission process causes the capacitance to vary with time. The signal profile of this transient capacitance depends on the carrier emission rates and the number of traps.

The rectangular injection pulse is shown in Fig. 2.3(b). V_R is the quiescent reverse-bias voltage, which was set at a value corresponding to a band bending of Ψ_B (Ψ_B is the energy difference between the E_F and intrinsic Fermi-level (E_i)) [6]. V_P is the pulse height, and V_{FB} is the flat band voltage. V_{AP} is the voltage representing the strength of accumulation, which is an important parameter for the BT analysis, because V_{AP} dominates the density of the majority carriers at the position near to the GeO_2/Ge interface. Therefore, we defined the pulse intensity as $\mathcal{E}_{AP} = V_{AP}/\text{EOT}$, where EOT is the equivalent oxide thickness. The frequency f and pulse width t_w are also important parameters for selecting the observed BT position (depth of z_0 , measured from the GeO_2/Ge interface) and for filling the majority carriers into BTs, respectively. In this study, f was set to be in a range of 10 to 1000 Hz. This frequency range corresponds to the z_0 ranges of 0.41-0.34 nm and 3.37-2.83 nm for p-MOSCAPs and n-MOSCAPs, respectively. The details about the calculation will be explained later. Since the z_0 range for p-MOSCAPs is too small, depth profiling of N_{bt} for p-MOSCAPs is not meaningful. Calculation details of D_{it} and N_{bt} are illustrated in sections 2.3.1 and 2.3.2, respectively.

2.3.1 D_{it} evaluation using DLTS

The expression for obtaining the $D_{it}(E)$ for MOSCAP was deduced from the following analytical procedures. The relation between the V_G and depletion width (W_d) for MOSCAP is given by V_G

$$V_G = q \int_0^{W_d(t)} \left(\frac{1}{C_{ox}} + \frac{x}{\epsilon_0 \epsilon_s} \right) N_A dx - \frac{q}{C_{ox}} \int_{E_{F1}}^{E_{F2}} D_{it}(E) e^{-\frac{t}{\tau_{it}(E)}} dE, \quad (2.8)$$

where q is the elementary charge, $W_d(t)$ is the depletion width at time t , ϵ_s is the dielectric constant of semiconductor, E_{F1} and E_{F2} are the Fermi levels for holes at the interface at the end of the capture process and in the emission process, respectively, and $\tau_{it}(E)$ is the emission time constant of hole from interface states at an energy position of E . As with carrier emission from bulk trap, carrier emission from the interface state is also a thermally activated process, and τ_{it} and emission rate $e_{it,p}$ are given by

$$\frac{1}{\tau_{it}} = e_{it,p} = N_v \sigma_{it,p} v_{th,p} e^{-\frac{E-E_V}{kT}}, \quad (2.9)$$

where $\sigma_{it,p}$ is the hole capture cross section of IT, and E is the energy level of interface state.

From the relation between $W_d(t)$ at time t and $W_d(t)$ at infinite time in Eq. (2.8), the following expression can be obtained:

$$\int_{W_d(\infty)}^{W_d(t)} \left(\frac{1}{C_{ox}} + \frac{x}{\epsilon_0 \epsilon_s} \right) N_A dx = \frac{1}{C_{ox}} \int_{E_{F1}}^{E_{F2}} D_{it}(E) e^{-e_{it,p}(E)t} dE. \quad (2.10)$$

The relation between the measured capacitance $C(t)$ and $W_d(t)$ is given by

$$\frac{1}{C(t)} = \frac{1}{C_{ox}} + \frac{W_d(t)}{\epsilon_0 \epsilon_s}. \quad (2.11)$$

The left term in Eq. (2.10) is given by

$$\int_{W_d(\infty)}^{W_d(t)} \left(\frac{1}{C_{ox}} + \frac{x}{\varepsilon_0 \varepsilon_s} \right) N_A dx = \frac{N_A \varepsilon_0 \varepsilon_s}{2} \left(\frac{1}{C(t)} - \frac{1}{C(\infty)} \right) \left(\frac{1}{C(t)} + \frac{1}{C(\infty)} \right). \quad (2.12)$$

Thus, the following expression can be deduced:

$$\frac{\Delta C(t)}{C^3(\infty)} = -\frac{1}{\varepsilon_0 \varepsilon_s N_A C_{ox}} \int_{E_{F1}}^{E_{F2}} D_{it}(E) e^{-e_{it,p}(E)t} dE, \quad (2.13)$$

where $\Delta C(t) = C(t) - C(\infty)$. Because $dE = -(kT/e_{it,p}) de_{it,p}$,

$$\frac{\Delta C(t)}{C^3(\infty)} = -\frac{kT}{\varepsilon_0 \varepsilon_s N_A C_{ox}} \int_0^\infty \frac{D_{it} e^{-e_{it,p}(E)t}}{e_{it,p}} de_{it,p}. \quad (2.14)$$

Equations (2.9) and (2.14) are the basic equations for the transient capacitance attributed to hole emission from ITs in the MOS structure.

In the case of our lock-in DLTS, which was synchronized to the bias pulse sequence having a wave function with time period $T_p (=1/f)$, the lock-in function $\Phi(x)$ for an exponential decay signal is given by

$$\Phi(x) = \left(\frac{e^{-\frac{x}{20}}}{x} - \frac{e^{-\frac{x}{2}}}{x} + \frac{e^{-\frac{x}{2}}}{20} \right) \left(1 - e^{-\frac{x}{2}} \right), \quad (2.15)$$

and

$$x = \frac{T_p}{\tau_{it}} = \frac{e_{it,p}}{f}. \quad (2.16)$$

The function $\Phi(x)$ had a peak when $x = 2.17$, whose value was 0.18. The half-maximum of $\Phi(x)$ was 0.09, the values of which were $x_1 = 0.5$ and $x_2 = 7.5$, which corresponded to $E_1 = E_v + kT \ln [N_v \sigma_{it,p} v_{th,p} / (0.5f)]$ and $E_2 = E_v + kT \ln [N_v \sigma_{it,p} v_{th,p} / (7.5f)]$, respectively.

The details of lock-in function are discussed in Appendix.

The difference ΔE between E_1 and E_2 is given by $\Delta E = kT \ln(7.5/0.5) = kT \ln(15) = 2.7kT$, which is within $3kT$. Because $D_{it}(E)$ is assumed to vary slowly in the energy range of $3kT$ around E , the term $D_{it}(E)$ can be taken out from the integral of Eq. (2.14), which is represented by

$$\frac{\Delta C(t)}{C^3(\infty)} = -\frac{kTD_{it}}{\varepsilon_0 \varepsilon_s N_A C_{ox}} \int_{0.5f}^{7.5f} \frac{e^{-e_{it,p}(E)t}}{e_{it,p}} de_{it,p}. \quad (2.17)$$

Thus, in the case of lock-in DLTS, Eq. (2.17) can be given as

$$\frac{\Delta C}{C^3(\infty)} = -\frac{kTD_{it}}{\varepsilon_0 \varepsilon_s N_A C_{ox}} \int_{0.5}^{7.5} \frac{\Phi(x)}{x} dx. \quad (2.18)$$

When a factor A is defined as $A = \int_{0.5}^{7.5} \frac{\Phi(x)}{x} dx$, A is numerically calculated as 0.4. If the capture cross section of the hole does not strongly depend on E , the energy level position E is deduced from Eq. (2.9) as:

$$E = E_v + kT \ln \left[N_v \sigma_{it,p} v_{th,p} / (2.17 f) \right]. \quad (2.19)$$

According to Eq. (2.19), the energy distribution of the IT signal can be obtained by scanning f or T . Since f is limited by the DLTS system and it is nature logarithm, scanning f provides very limited range of energy distribution. Therefore, in this study, we fixed f at 10 Hz and scanned T for D_{it} measurement. The $D_{it}(E)$ is given by:

$$D_{it} = \frac{|\Delta C| C_{ox} \varepsilon_0 \varepsilon_s N_A}{A C^3(\infty) kT}. \quad (2.20)$$

The $\sigma_{it,p}$ is the same as that in the capture process. When we consider the effect of capture process. The obtained DLTS signal can be rewritten as

$$\frac{\Delta C}{C^3(\infty)} = \frac{AD_{it}kT}{C_{ox}\epsilon_0\epsilon_s N_A} \left(1 - e^{-\frac{t_w}{\tau_c}}\right), \quad (2.21)$$

where τ_c is the capture time constant given by

$$\tau_c = \frac{1}{\sigma_{it,p} v_{th,p} N_A}. \quad (2.22)$$

which can be measured by monitoring the t_w dependence of DLTS response. The filling pulse duration dependence of DLTS signal $\Delta C/C^3(\infty)$ is shown in Fig. 2.4. Since τ_c is very small, a low-doped substrate is recommended for $\sigma_{it,p}$ measurement. Instead of capture, emission is the rate limiting process, and D_{it} can be correctly measured by applying a sufficient long t_w .

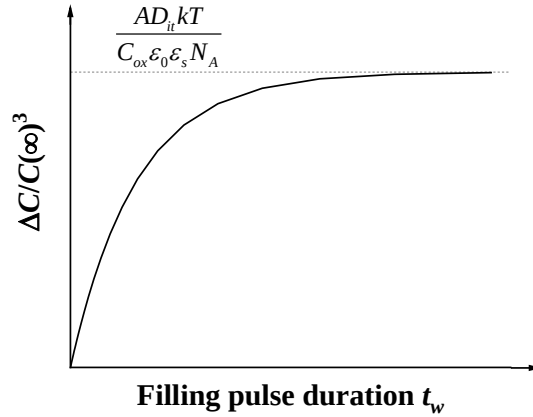


FIG. 2.4 Filling pulse duration dependence of DLTS signal during capture process.

2.3.2 N_{bt} evaluation using DLTS

Analysis of the BT density is similar to that of the interface state density. First, note that the BT density (n_{bt}), and N_{bt} have units of cm^{-2} and cm^{-3} , respectively.

$$\frac{1}{\tau_t(E_t, z)} = e_t(E_t, z) = \alpha e^{-az} \quad \text{and} \quad a = 2 \left[\frac{(2m_i^* E_t)^{1/2}}{\hbar} \right], \quad (2.23)$$

where τ_t and e_t are the time constant and the emission rate of tunneling process, respectively, m_i^* is the insulator effective mass, $\hbar$ is the reduced Planck constant, α is the pre-exponential factor of $\sim 2 \times 10^{12} \text{ s}^{-1}$ having the physical meaning of tunneling probability, and E_t is the tunneling barrier height having the maximum of the valence band offset E_{tp} for p-MOSCAP or the conduction band offset E_{tn} for n-MOSCAP. The details will be discussed later. The band offset of GeO_2/Ge is shown in Fig. 2.5 [7]. Here, $e_t(E_t, z)$ depends on only z . The V_G is given by

$$V_G = q \int_0^{w(t)} \left(\frac{1}{C_{ox}} + \frac{x}{\epsilon_0 \epsilon_s} \right) N_A dx - \frac{q}{C_{ox}} \int_0^z N_{bt}(z) e^{-e_t(z)t} dz. \quad (2.24)$$

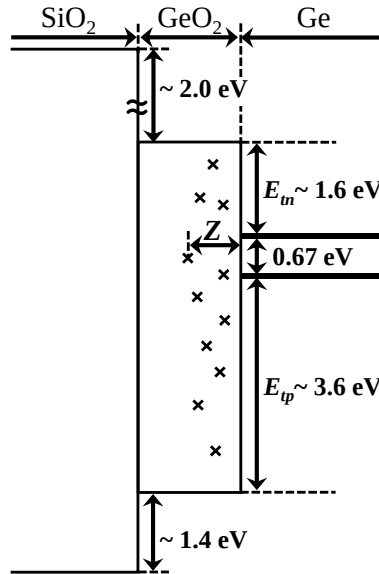


FIG. 2.5 Band diagram of the $\text{SiO}_2/\text{GeO}_2/\text{Ge}$ structure [7].

Carrier emission from the border trap at a distance z is a tunneling process, which is independent on T . Similar to the D_{it} calculation, the following expression can be deduced:

$$\frac{\Delta C(t)}{C^3(\infty)} = -\frac{1}{\varepsilon_0 \varepsilon_s N_A C_{ox}} \int_0^z N_{bt}(z) e^{-e_t(z)t} dz. \quad (2.25)$$

When the N_{bt} is localized at a distance of z_0 , Eq. (2.25) is expressed by

$$\frac{\Delta C(t)}{C^3(\infty)} = -\frac{N_{bt}(z_0) \Delta z}{\varepsilon_0 \varepsilon_s N_A C_{ox}} e^{-e_t(z_0)t} = -\frac{n_{bt}(z_0)}{\varepsilon_0 \varepsilon_s N_A C_{ox}} e^{-e_t(z_0)t}. \quad (2.26)$$

For this case, lock-in DLTS is expressed by

$$\frac{\Delta C(t)}{C^3(\infty)} = -\frac{n_{bt}(z_0)}{\varepsilon_0 \varepsilon_s N_A C_{ox}} \Phi(x), \quad (2.27)$$

$$n_{bt} = \frac{|\Delta C| C_{ox} \varepsilon_0 \varepsilon_s N_A}{C^3(\infty)} \left(\frac{1}{0.18} \right), \quad z_0 = \frac{\hbar}{2\sqrt{2m_i^* E_t}} \ln \left(\frac{\alpha}{2.17 f} \right) = \frac{1}{a} \ln \left(\frac{\alpha}{2.17 f} \right). \quad (2.28)$$

Both the effective hole mass ($\sim 10 m_e$) and effective electron mass ($\sim 0.43 m_e$) in α -quartz GeO_2 have been calculated with the Heyd-Scuseria-Ernzerhof (HSE) hybrid functional and reported by A. V. Shaposhnikov *et al* [8]. Accordingly, the $1/a$ was calculated as $\sim 1.61 \times 10^{-11}$ m (0.0161 nm), when $m_e = 9.1 \times 10^{-31}$ kg, $\hbar = 1.05 \times 10^{-34}$ J s, $E_t \sim E_{tp} = 3.6$ eV (5.8×10^{-19} q). It should be noted that the $1/a$ was calculated as $\sim 1.18 \times 10^{-10}$ m (0.118 nm) for n-Ge MOSCAP, when $E_t \sim E_{tn} = 1.6$ eV (2.6×10^{-19} q) [7].

The n_{bt} distribution can be obtained similar to the D_{it} calculation. The half-maximum positions of $\Phi(x)$ are given by $z_1 = \frac{1}{a} \ln[\alpha/(0.5f)]$ and $z_2 = \frac{1}{a} \ln[\alpha/(7.5f)]$, respectively.

The difference Δz between z_1 and z_2 is given by $\Delta z = (1/a) \ln(7.5/0.5) = (1/a) \ln(15)$,

which is within a very narrow range. Because $N_{bt}(z)$ was assumed to vary slowly in the small range around z_0 , the term N_{bt} can be taken out from the integral of Eq. (2.25). Because

$$dz = -de_t / (ae_t),$$

$$\frac{\Delta C(t)}{C^3(\infty)} = -\frac{N_{bt}}{a\epsilon_0\epsilon_s N_A C_{ox}} \int_{0.5f}^{7.5f} \frac{e^{-e_i(z)t}}{e_t} de_t, \quad (2.29)$$

Thus, in the case of lock-in DLTS, Eq. (2.29) can be given by

$$\frac{\Delta C(t)}{C^3(\infty)} = -\frac{N_{bt}}{a\epsilon_0\epsilon_s N_A C_{ox}} \int_{0.5}^{7.5} \frac{\Phi(x)}{x} dx. \quad (2.30)$$

Also, we can deduce the $N_{bt}(z_0)$ as the following:

$$N_{bt}(z_0) = \frac{|\Delta C| C_{ox} \epsilon_0 \epsilon_s N_A a}{A C^3(\infty)}, \quad (2.31)$$

where A is 0.4.

The border trap position z_0 is deduced from Eq. (2.23) as the following expression:

$$z_0 = \frac{1}{a} \ln\left(\frac{\alpha}{2.17f}\right) = \frac{\hbar}{2\sqrt{2m_i^* E_t}} \ln\left(\frac{\alpha}{2.17f}\right). \quad (2.32)$$

Depth profiling can be obtained by changing f , and the maximum f of our DLTS system is 2500 Hz. However, in order to keep the accuracy of measurement, t_w is limited to be less than or equal to $T_p/20$. Therefore, when t_w is set to be 50 μs , the maximum f is 1000 Hz. For p-MOSCAP, when $f = 10, 30, 100, 300$ and 1000 Hz, $z_0 = 0.41, 0.39, 0.37, 0.36$ and 0.34 nm, respectively. Since the z_0 range is too small, depth profiling of N_{bt} for p-MOSCAP is not meaningful. For n-MOSCAP ($\alpha \sim 6 \times 10^{13} s^{-1}$), when $f = 10, 30, 100, 300$ and 1000 Hz, $z_0 = 3.37, 3.24, 3.10, 2.97$ and 2.83 nm, respectively. According to Eq. (2.32), the spatial and energy distribution of the BTs in a n-MOSCAP which can be detected by lock-in DLTS is shown in Fig. 2.6. The blue curve refers to measurement condition $f = 10$ Hz while the red curve refers to measurement condition $f = 1000$ Hz. In other words, only the BTs located in between blue and red curves can be detected due to the limitation of the DLTS system (when t_w is set to be 50 μs).

When we consider the band bending in capture process, the energy level of filled BT depends on the electric field strength in GeO_2 $\mathcal{E}_{\text{GeO}_2}$ and tunneling depth z . The relation is as follows:

$$E(d) = E_v - q \mathcal{E}_{\text{GeO}_2} z \text{ for p-MOSCAP and } E(d) = E_c + q \mathcal{E}_{\text{GeO}_2} z \text{ for n-MOSCAP, (2.33)}$$

where $\mathcal{E}_{\text{GeO}_2} = \mathcal{E}_{\text{AP}} \epsilon_{\text{SiO}_2} / \epsilon_{\text{GeO}_2}$ in the case of $\text{SiO}_2/\text{GeO}_2/\text{Ge}$ gate stacks, and ϵ_{SiO_2} and ϵ_{GeO_2} are dielectric constant of SiO_2 and GeO_2 , respectively. Therefore, with increasing filling pulse, the BTs at deeper position and shallower-energy level can be filled and detected. For example, in the case of $\mathcal{E}_{\text{AP}} = 2 \text{ MV/cm}$, only the area under dash line in Fig. 2.6 can capture electrons, which means only the BTs in the green area can be detected by lock-in DLTS.

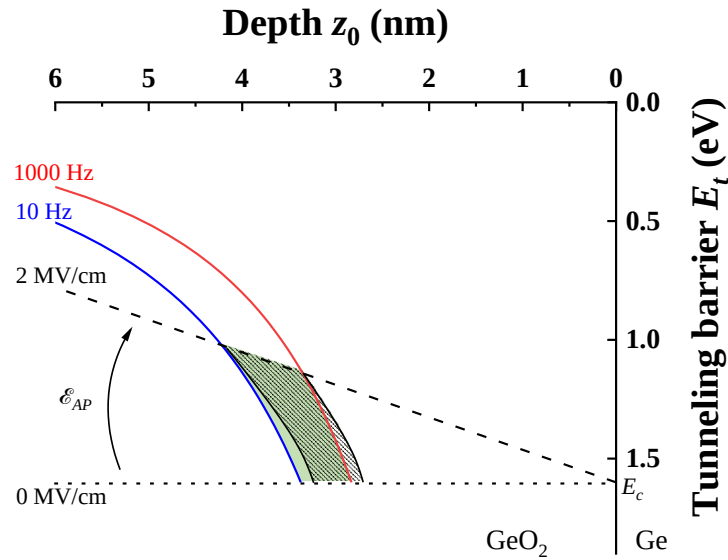


FIG. 2.6 Range of energy and depth of BT in n-MOSCAP detected by lock-in DLTS (green area). Blue and red lines are based on the BT emission equation Eq. (2.32) and the lock-in DLTS. Hatched area is the result in the same case but considers the energy dependence of pre-exponential factor α . Dot line and Dash line are the maximum energy level of capture when the filling electric field $\mathcal{E}_{\text{AP}}$ is 0 and 2 MV/cm, respectively.

The pre-exponential factor α is dependent on tunneling barrier E_t and depth tunneling-emission probability for p-MOSCAP, is as follows:

$$\alpha = \frac{\hbar}{36m_p^*} \left(\frac{\pi}{2} \right)^5 \frac{E_t}{E_t + (m_p^*/m_i^*)(E_{tp} - E_t)} \frac{[2m_p^*(E_{tp} - E_t)]^{1/2}}{\hbar z} \times \left\{ 1 - \exp \left[-\frac{z}{\hbar} \left[2 \frac{(m_p^*)^2}{m_i^*} \frac{(E_{tp} - E_t)^2}{E_t} \right]^{1/2} \right] \right\} \quad [9]. \quad (2.34)$$

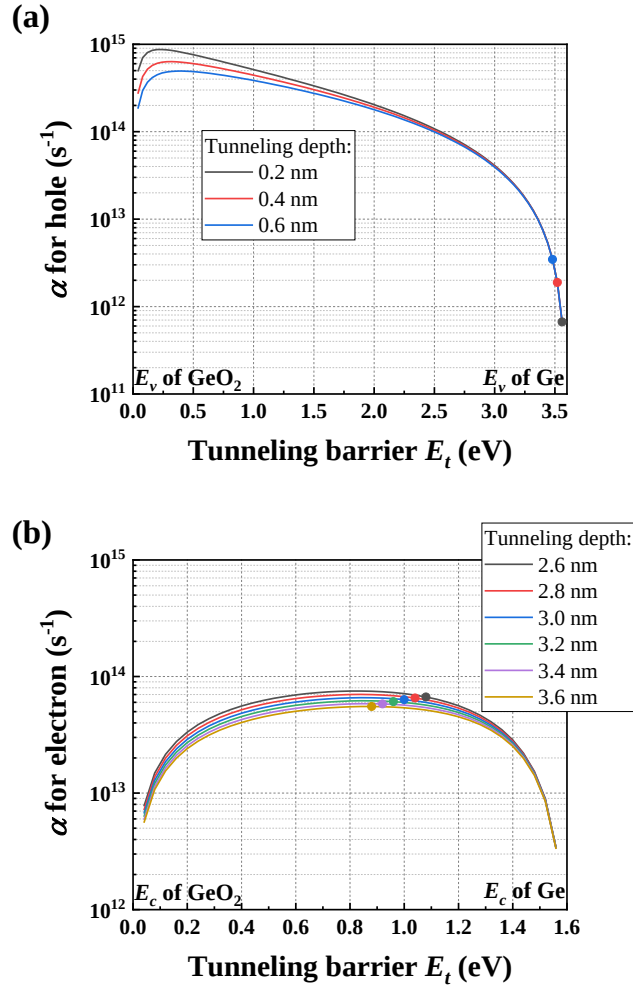


FIG. 2.7 Evolution of α , the tunneling-emission probability, as a function of energy level of defects with several depths in GeO₂ of (a) p-MOSCAP and (b) n-MOSCAP. The colored dots are the results when the band bending of $\mathcal{E}_{AP} = 2$ MV/cm at each depth is taken into account.

For n-MOSCAP, we can simply replace the term E_{tp} and m_p^* in Eq. (2.34) with E_{tn} and semiconductor effective electron mass m_n^* , respectively. Figure 2.7 (a) and (b) show α as a function of tunneling barrier in GeO₂ with several tunneling depth for (a) p- and (b) n-MOSCAP, respectively. Here, m_p^* and m_n^* for Ge are $0.38 m_e$ and $0.22 m_e$, respectively. Since the measuring depth for p-MOSCAP is approximately 0.4 nm, where band bending is still not serious ($E_t \sim 3.54$ eV), α is $\sim 2 \times 10^{12} \text{ s}^{-1}$ (red dot in Fig. 2.7 (a)). In the case of n-MOSCAP with measuring condition $\mathcal{E}_{AP} = 2 \text{ MV/cm}$, the band bending at the measuring depth (2.8~ 3.4 nm) during capture process is not negligible. When the band bending is taken into account, the minimum E_t (~ 1.0 eV) dependent on each tunneling depth corresponds to $\alpha \sim 6 \times 10^{13} \text{ s}^{-1}$. Since α strongly depends on tunneling barrier around $E_t \sim 1.5$ eV, the green area in Fig. 2.6 should be corrected into hatched area considering the energetically dependence of α .

2.3.3 Bias selecting

Since the minority carrier can interfere the DLTS measurement on MOSCAP, it is essential to prevent from minority carrier formation. Therefore, the measurement has to be conducted at low temperature, and the V_R should be carefully selected. In this study, the V_R is set to a value corresponding to a band bending of Ψ_B . This band bending condition can be found by adjusting the bias to reverse capacitance $C(\infty) = C_s$, and C_s is given by

$$C_s = \frac{C_{ox} C_{dep}}{C_{ox} + C_{dep}}, \quad (2.35)$$

where C_{dep} is the capacitance of depletion region. C_{ox} and C_{dep} is given as follows:

$$C_{ox} = \frac{\epsilon_0 \epsilon_{SiO_2}}{\text{EOT}} \quad (2.36)$$

and
$$C_{dep} = \frac{\epsilon_0 \epsilon_{Ge}}{W_d}. \quad (2.37)$$

W_d at the condition of band bending Ψ_B is given by

$$W_d = \sqrt{\frac{2\epsilon_0 \epsilon_s \Psi_s}{qN_A}}, \quad (2.38)$$

and Ψ_B is given by

$$\Psi_B = 0.5E_g - (E_F - E_v) = 0.5E_g - kT \ln\left(\frac{N_v}{N_A}\right), \quad (2.39)$$

where E_g is the band gap.

2.4 Lock-in DLTS

In this study, all DLTS measurement were performed using a SEMILAB DLS83D system with a lock-in DLTS. The capacitance meter is a 1 MHz phase sensitive rectifier. Figure 2.8 shows how the lock-in integrator processed the transient capacitance [10]. When Pulse voltage train is applied (Fig. 2.8(a)), capacitance transient is obtained (Fig. 2.8(b)). After multiplied with the lock-in function (Fig. 2.8(c)), the exponential decay capacitance transient becomes like Fig 2.8(d). The integration of Fig 2.8(d) is the Eq. (2.15), which corresponds to a rate window shown in Fig. 2.9. Most of signals are from the range of $e_t/f = 0.5$ to 7.5, which means D_{it} and N_{bt} are mostly calculated from this region. According to the emission rate of ITs and BTs (Eq. (2.9) and (2.23)), the ranges are

$$\Delta E = kT \ln\left(\frac{7.5}{0.5}\right) \quad (2.40)$$

for ITs, and

$$\Delta z = \frac{1}{a} \ln\left(\frac{7.5}{0.5}\right) \quad (2.41)$$

for BTs. Consequently, D_{it} and N_{bt} show different units ($\text{eV}^{-1} \text{cm}^{-2}$ and cm^{-3} , respectively).

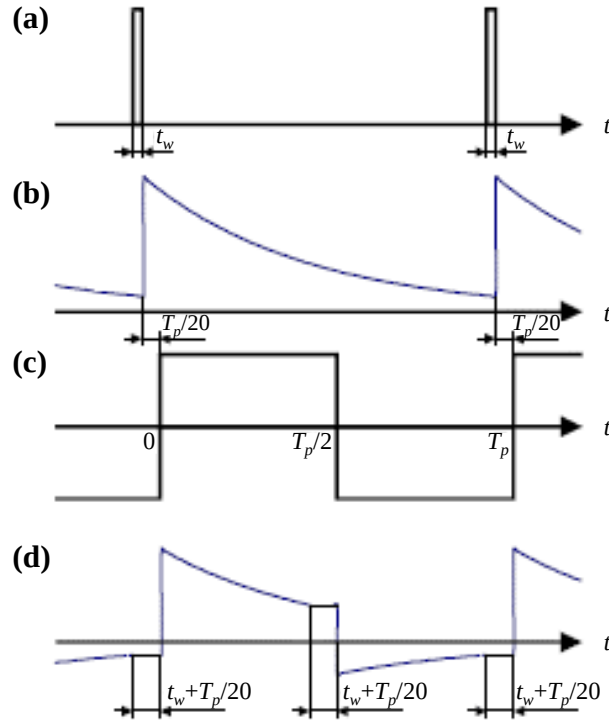


FIG. 2.8 (a) Pulse voltage train, (b) capacitance transient, (c) lock-in function and (d) capacitance transient multiplied with the lock-in function [10].

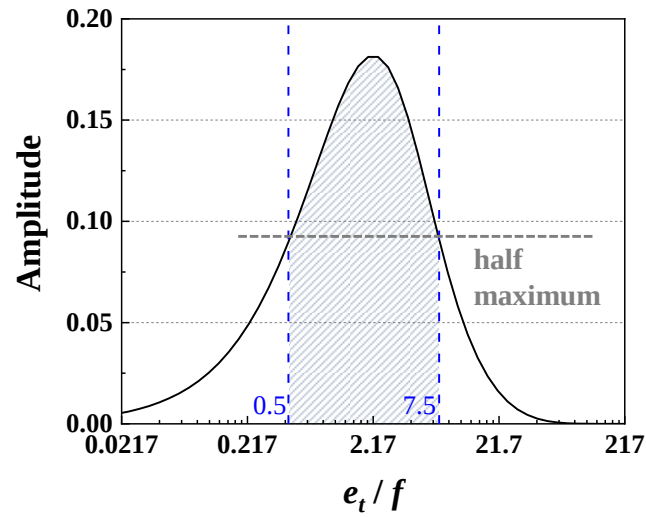


FIG. 2.9 An emission rate window of the lock-in DLTS.

2.5 Summary of this chapter

Principle of DLTS is described and the calculation details of different traps at different position of MOS structures are shown. Even though DLTS can help evaluate traps densities, different kind of traps direct to different equations according to their nature. As a result, it is crucial to distinguish the source of DLTS signal so that the trap density will not be miscalculated. The details of signal separation will be discussed in the next chapter.

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Chapter 3 Interface trap and border trap evaluation for SiO₂/GeO₂/Ge gate stacks using DLTS [1–3]

3.1 Introduction

Although a GeO₂ interlayer is effective in reducing ITs, the fabrication of high-performance Ge MOSFETs is still challenging owing to the defects in the gate stacks and the parasitic resistance of the source/drain contacts, particularly for Ge n-MOSFETs [4,5]. Even though a high mobility can sometimes be achieved, the mobility drop drastically in the high effective field region [5–7]. This may be because of the substrate quality, the interface roughness and the BTs in the oxide layers [8–10]. A large amount of BTs lead to serious problems such as a degraded channel mobility and unstable threshold voltage [11].

To improve the performance of Ge MOSFETs, the establishment of a BT evaluation method is necessary. In chapter 2, the calculation of N_{bt} in GeO₂/Ge structure using DLTS has been introduced. In this chapter, a practical BT evaluation for SiO₂/GeO₂/Ge gate stacks grown by thermal oxidation and plasma oxidation will be presented. The effect of Al post metallization annealing (PMA) on the quality of the gate stacks will be also discussed.

In section 3.2, the procedures of MOSCAPs fabrication are described. In section 3.3, the electrical properties of thermally grown p-MOSCAP without Al-PMA are reported. The DLTS signals and the signal identifications of IT and BT are presented, and the result of D_{it} are determined and shown. In section 3.4-3.6, N_{bt} of all MOSCAPs are presented, and the depth profiling of N_{bt} for PTO n-MOSCAPs is also performed. Section 3.7 presents the summary of this chapter.

3.2 Sample fabrication

Both p- and n-type (100) Ge substrates with respective doping concentrations of 2.3×10^{16} and $9.3 \times 10^{15} \text{ cm}^{-3}$ were used. After the substrates were cleaned by dilute HF solution and rinsed with deionized water, an ultrathin $\text{SiO}_2/\text{GeO}_2$ BLP was performed by radio-frequency (rf) sputtering at 350 °C [12]. Here, the thicknesses of both SiO_2 and GeO_2 layers were ~ 1 nm. Next, post-passivation thermal oxidation (PTO) was performed at 550 °C for 15 min or 425 °C for 9 h in ambient O_2 . Then, 14-nm-thick SiO_2 was deposited on both samples by rf-sputtering at room temperature (RT), followed by post-deposition annealing (PDA) at 400 °C for 30 min in ambient N_2 . The purpose of forming this thick SiO_2 layer is to prevent the influence of leakage current on carrier capture process through BT. After an Al layer was deposited on the SiO_2 surface by thermal evaporation, an optional Al-PMA was carried out at 300 °C for 30 min in ambient N_2 . Finally, the electrodes were patterned with an area of $5.66 \times 10^{-4} \text{ cm}^2$, and a back-contact formation by an In-Ga alloy was performed. The EOTs of the gate dielectric films with PTO at 550 and 425 °C were approximately 19.5 and 16.8 nm, which implied GeO_2 thicknesses of 6.0 and 3.3 nm, respectively. The fabrication process is shown in Fig. 3.1, and the sputtering parameters for BLP and SiO_2 deposition are listed in Table 3.1.

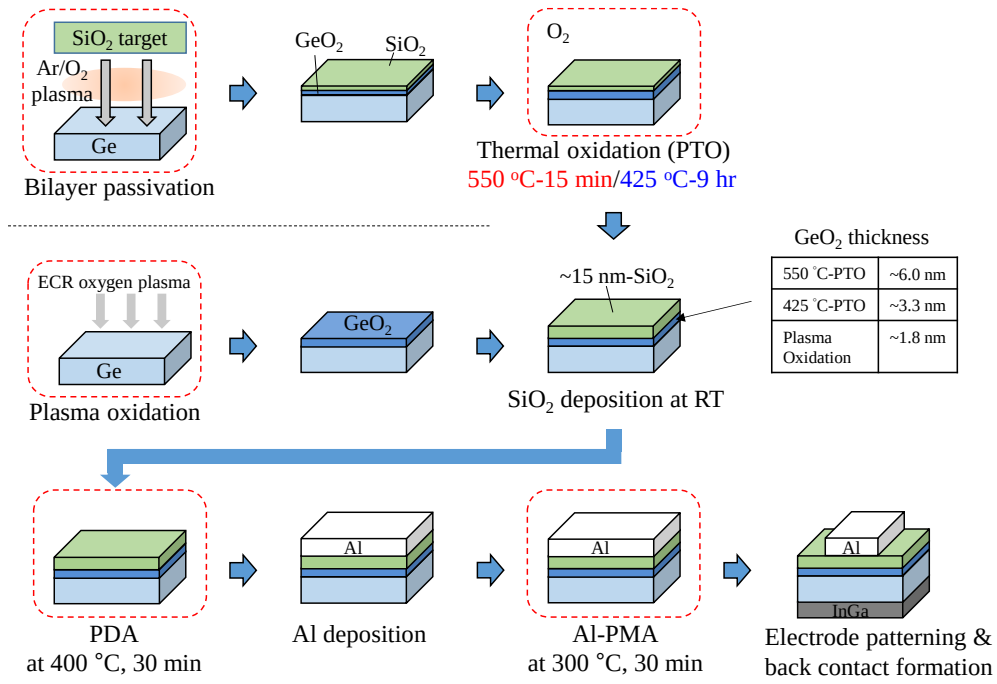


FIG. 3.1 Fabrication process of MOSCAPs.

TABLE 3.1 Sputtering parameters for BLP and SiO_2 deposition.

Parameter	BLP	SiO_2 deposition
rf power P_{rf} (W)	13	50
Ar flow rate (sccm)	20	20
O_2 flow rate (sccm)	0.2	--
Pressure (Pa)	0.96	0.95
Deposition rate (nm/min)	0.11	2.55
Temperature ($^\circ\text{C}$)	350	RT
Time	9 min 6 sec	5 min 29 sec

Other MOSCAPs were also fabricated for comparison with PTO MOSCAPs. After chemical cleaning, both p- and n-type Ge substrates were plasma oxidized by electron cyclotron resonance (ECR) at 130 °C with a microwave power of 300 W and Ar/O₂ flow rates of 16/8 sccm for 3 min. Then, 15-nm-thick SiO₂ was deposited by rf-sputtering. The parameters of ECR plasma oxidation are listed in Table 3.2. The residual processes were the same as those of PTO MOSCAPs. The EOTs were approximately 16.2 nm, which implied a GeO₂ thickness of 1.8 nm. Actually, this was the maximum thickness that could be obtained for a GeO₂ layer fabricated under above-mentioned conditions owing to the nature of ECR plasma oxidation. The sample fabrication process is also shown in Fig. 3.1. Both D_{it} and N_{bt} were characterized using DLTS, and the pulse frequency of 10 Hz was set except for the depth profiling of N_{bt} in n-MOSCAPs (see section 2.3) [1–3].

TABLE 3.2 Parameters for ECR plasma oxidation.

Parameter	ECR plasma oxidation
Microwave power P_{μ} (W)	300
Ar flow rate (sccm)	16
O ₂ flow rate (sccm)	8
Pressure (Pa)	0.15
Temperature (°C)	130
Time	3 min

In order to clarify the main composition of this ECR plasma oxidized film, x-ray photoelectron spectroscopy (XPS) measurement with a monochromatic Al K- α X-ray source has been carried out, as shown in Fig. 3.2. An XPS result of thermally grown GeO₂/Ge structure with a GeO₂

thickness of 1.5 nm is also shown for comparison. Although the peak position of Ge oxide is slightly different between these two samples, there is no doubt that the main product of ECR plasma oxidation is GeO_2 . Note the binding energy of Ge^{2+} (GeO) is 31.0 eV, where no clear signal was observed.

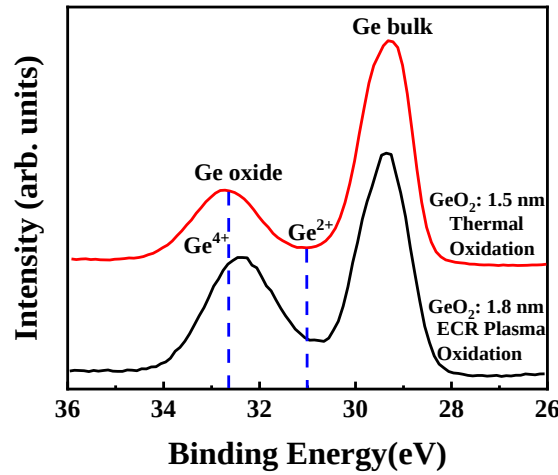


FIG. 3.2 Ge 3d XPS spectra for thermally grown and ECR plasma oxidized GeO_2 films.

3.3 Electrical properties, DLTS signal, D_{it}

3.3.1 Electrical properties for $\text{SiO}_2/\text{GeO}_2/\text{Ge}$ gate stacks grown by PTO

To clarify the electrical properties of MOSCAPs, both C - V and current-voltage (I - V) characteristics were measured. Figure 3.3 shows typical results for 550 °C PTO p- and n-MOSCAPs without Al-PMA. The hysteresis and frequency dispersion in the C - V curves were small. The obvious V_{FB} shift originates from the unintentional formation of dipoles at the $\text{SiO}_2/\text{GeO}_2$ interface [13], and this shift was observed for all the MOSCAPs with more or less varied values. From the I - V results, current density (J) and effective electric field ($\mathcal{E}_{eff}$) were calculated, as shown in fig. 3.3 (c) and (d). The breakdown $\mathcal{E}_{eff}$ were 5.28 and 3.91 MV/cm for p- and n-MOSCAPs, respectively, which were high enough for DLTS measurement.

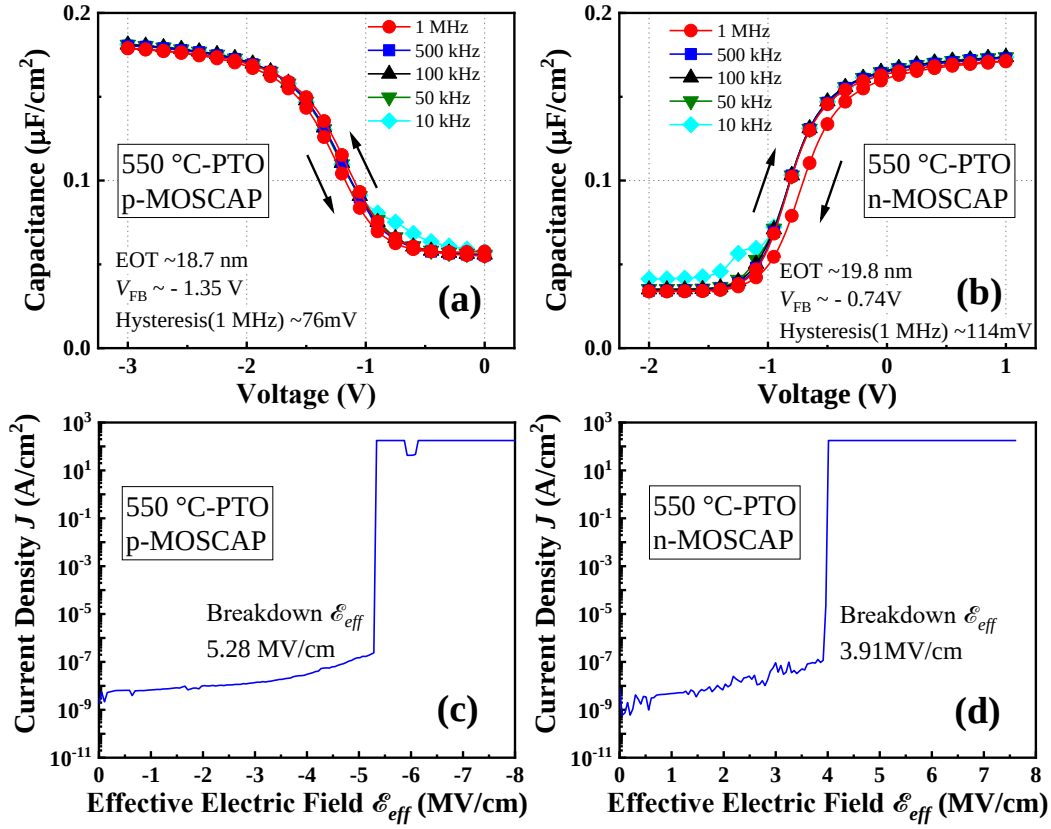


FIG. 3.3 C-V curves of 550 °C-PTO (a) p-MOSCAP and (b) n-MOSCAP without Al-PMA. I - V curves of 550 °C-PTO (c) p-MOSCAP and (d) n-MOSCAP without Al-PMA. All the C-V and I - V characteristics were measured at RT.

3.3.2 DLTS signal of SiO₂/GeO₂/Ge gate stacks grown by PTO

Since high-quality commercial Ge wafers were used in this study, the trap densities of impurities and crystalline defects are below the sensitivity of our DLTS system, which means the contribution of bulk traps to DLTS signals can be ignored in this case. However, the signal of ITs and BTs still have to be distinguished and separated, and then calculated using different equations as derived in chapter 2. Figure 3.4 shows the dependence of the DLTS signal intensity (I_{DLTS}) on t_w at different temperatures with different $\mathcal{E}_{\text{AP}}$. Pulse frequency was set to 10 Hz. Here, $\Delta C/C(\infty)^3$ was plotted as I_{DLTS} because both N_{bt} and D_{it} were proportional to $\Delta C/C(\infty)^3$. Because the capture

cross section σ of IT was in the range of 10^{-16} – 10^{-15} cm², the minimum t_w value of 2 μ s was sufficient to accomplish the capture process of IT [14]. Therefore, the increase in I_{DLTS} with increasing t_w arose from the increased number of carriers captured by BT. Note the increase in I_{DLTS} was quite small considering the more than three-order increase in t_w , which implied a very small σ of BT. This was reasonable because the carrier tunneling process governs the σ of BT [15]. The relatively faster increase in I_{DLTS} for n-Ge sample arose from the lower barrier height for electrons tunneling from Ge to GeO₂ [16,17]. The I_{DLTS} also depended on $\mathcal{E}_{AP}$ because the density of accumulated carriers is an important parameter for the capture process of BT owing to the small σ .

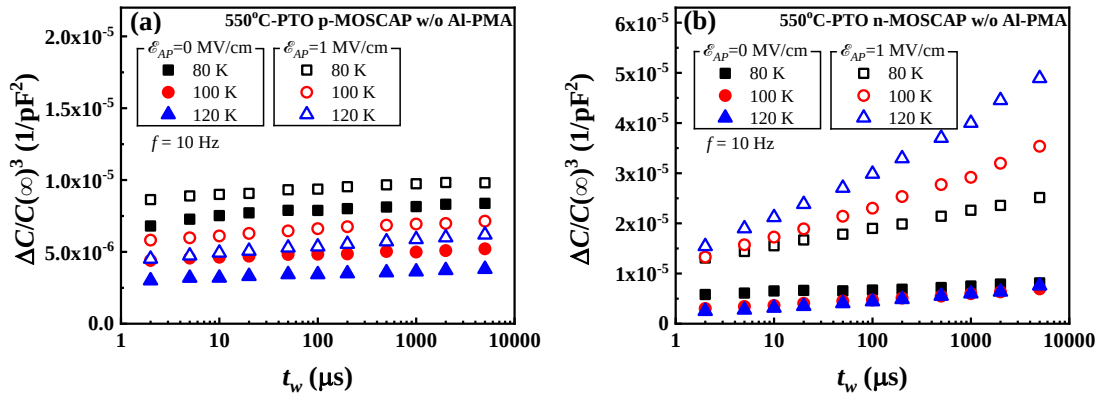


FIG. 3.4 I_{DLTS} dependence on t_w for (a) 550 °C-PTO p-MOSCAP and (b) 550 °C-PTO n-MOSCAP.

To determine the details of the capture process in the DLTS measurement, the dependence of I_{DLTS} on the injection pulse height with the maximum t_w of 5 ms was studied, as shown in Fig. 3.5. Taking the result of a p-MOSCAP at 80 K as an example, I_{DLTS} drastically increased when the pulse height was increased from 0 to 0.5 V. Note that 0.5 V was approximately the V_{FB} for this sample at 80 K. Therefore, this increase was dominated by the capture process of IT [14]. In the case of $V_P > 0.5$ V, namely where accumulation was established, the contribution of IT would be

saturated owing to the completion of IT capture. As a result, the increase in I_{DLTS} with $V_P > 0.5$ V was dominated by the slow capture process of BT. The two-step feature of the I_{DLTS} increase was less clear for an n-Ge sample owing to its small D_{it} value and relatively faster BT capture process.

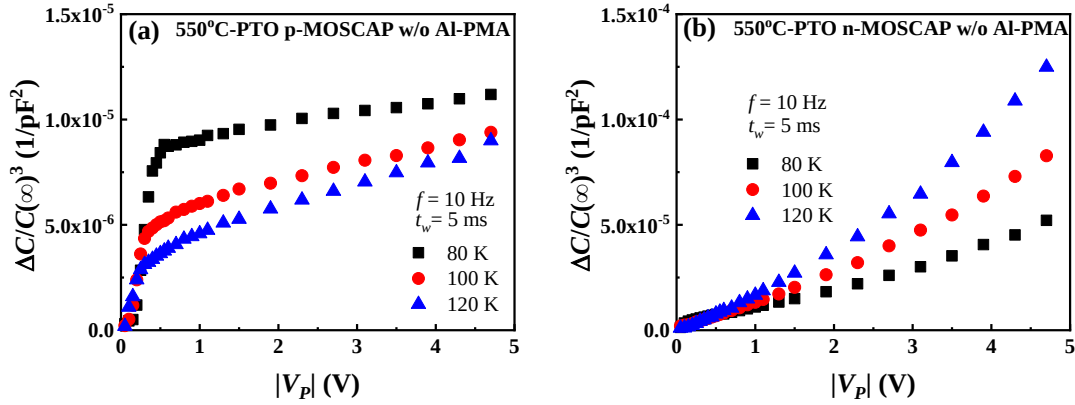


FIG. 3.5 I_{DLTS} dependence on V_P for (a) p-MOSCAP and (b) n-MOSCAP. Both samples are 550 °C PTO.

The I_{DLTS} did not saturate with increasing V_P , implying that the BTs at a deeper position and a shallower energy level were detected. This phenomenon can be explained by figure 3.6. The BTs below E_F captured electron during capture process, and then electrons emitted from these BTs during emission process. However, only the BTs at z_0 with the energy level very close to the conduction band edge of Ge could be detected when V_P was slightly higher than V_{FB} (detected BTs are highlighted in blue in Fig. 3.6(a)), which meant the band bending of GeO_2 layer is negligible. In Fig. 3.6(b), the strong $\mathcal{E}_{AP}$ caused an obvious band bending in GeO_2 layer, and the BTs with the energy level higher than the conduction band edge of Ge were also filled with electrons. Consequently, not only the BTs at z_0 but also BTs at deeper position with shallower-energy level can be detected. As a result, the I_{DLTS} did not saturate with increasing V_P . Based on

the nature of IT and BT, the DLTS signal under the weakest injection condition shown in Fig. 3.4 ($t_w = 2 \mu\text{s}$, $\mathcal{E}_{AP} = 0 \text{ MV/cm}$) was thought to be mainly contributed by IT, and these data were used to calculate D_{it} (see Section 2.3.1).

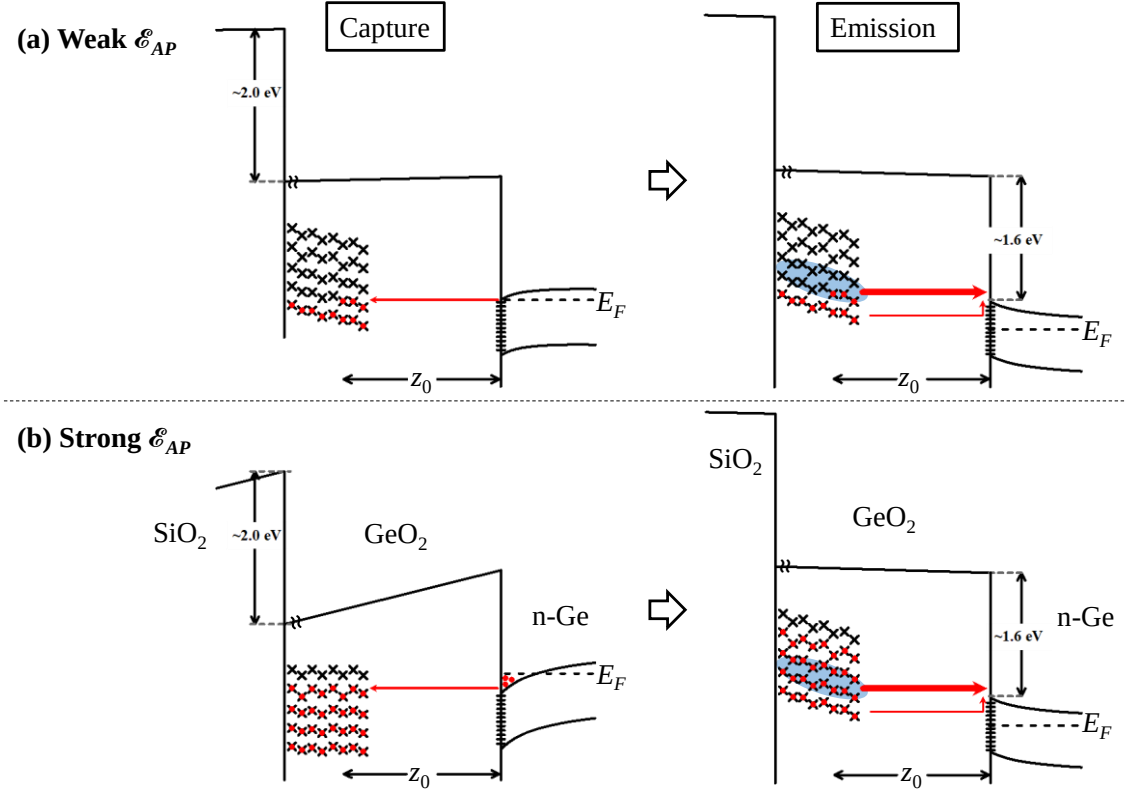


FIG. 3.6 Border traps in band diagrams of a $\text{SiO}_2/\text{GeO}_2/\text{Ge}$ n-MOSCAP with (a) weak $\mathcal{E}_{AP}$ and (b) strong $\mathcal{E}_{AP}$ during capture process. The detected border traps are highlighted in blue.

3.3.3 D_{it} evaluation of $\text{SiO}_2/\text{GeO}_2/\text{Ge}$ gate stacks using DLTS

Figure 3.7 shows the energy distribution of D_{it} for all the samples. Al-PMA is shown to be beneficial to passivate IT near the valence band, but not for those near the conduction band. Furthermore, the D_{it} of the 425°C -PTO samples were higher than that of the 550°C -PTO samples, and the D_{it} of MOSCAPs fabricated by ECR plasma oxidation was even higher than those of the PTO samples. This was reasonable because the quality of the GeO_2/Ge interface was sensitive to

the fabrication method as well as the temperature of the thermal treatment. Generally, a better quality of the GeO_2/Ge interface can be achieved under a higher temperature of the thermal treatment. The fabrication temperature of the 550 °C-PTO samples was the highest, while that of the ECR samples was the lowest. As a result, the ECR samples showed the worst interface quality. The interface quality of ECR samples may be improved by optimizing the condition of ECR plasma oxidation. However, this is beyond the scope of this study.

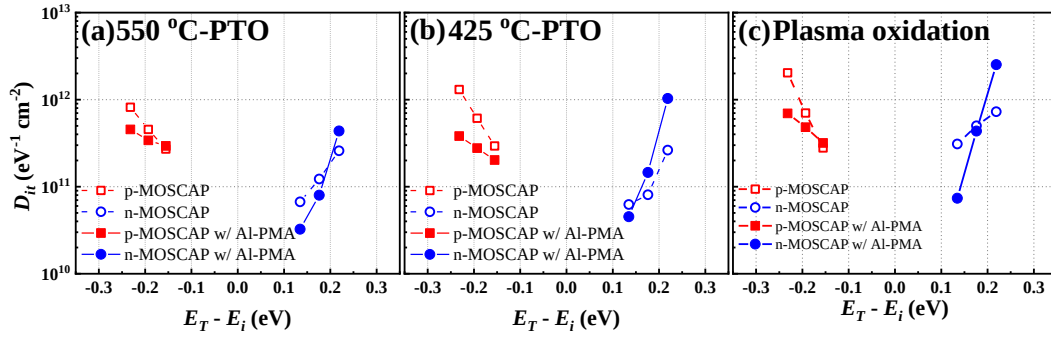


FIG. 3.7 Energy distribution of D_{it} measured by DLTS with pulse frequency 10 Hz and filling pulse duration 2 μs for the samples thermally oxidized at (a) 550 °C and (b) 425 °C, and (c) oxidized by plasma.

3.4 N_{bt} of p-MOSCAPs

After subtracting the IT signals from I_{DLTS} , N_{bt} were calculated (see Section 2.3.2). Figure 3.8 shows the temperature dependence of N_{bt} for p-MOSCAPs, measured under an f of 10 Hz, which corresponded to a BT position of 0.41 nm from the GeO_2/Ge interface. It was observed that the N_{bt} of the 425 °C-PTO p-MOSCAPs was higher than that of the 550 °C-PTO p-MOSCAPs. After Al-PMA, the N_{bt} s of both the 425 °C-PTO p-MOSCAPs and 550 °C-PTO p-MOSCAPs decreased to nearly the same level.

lower (< 55 meV) than the valence band edge of Ge, as demonstrated in Fig. 3.9. Because this energy difference was quite small, it could be concluded that Al-PMA was also effective for passivating the BTs at the energy levels near to the valence band. It is worth noting the negligible temperature dependence of N_{bt} s for the p-MOSCAPs. This implied that the detected BTs were irrelevant to the thermal emission process, which suggested that the energy level of those BTs was centralized at the position near to the valence band. The decreases in D_{it} and N_{bt} through Al-PMA were considered to be the main reasons why we could achieve a high mobility in the Ge p-MOSFETs [18].

3.5 N_{bt} of n-MOSCAPs

Figure 3.10 shows the temperature dependence of N_{bt} for n-MOSCAPs, measured under an f of 10 Hz, which corresponded to a BT position of 3.37 nm from the GeO_2/Ge interface. Similar N_{bt} results were observed for both the 425 °C-PTO and 550 °C-PTO n-MOSCAPs. There was no clear difference of N_{bt} between the samples with and without Al-PMA, and the N_{bt} values were in the same range as those obtained for the p-MOSCAPs with Al-PMA (see Fig. 9). The relatively stronger temperature dependence of N_{bt} implied that a thermal emission process was involved in the overall emission process from BTs. As a result, the energy of the measured BTs should be distributed in a certain range.

Figure 3.11 shows the N_{bt} depth profiling of an n-MOSCAP, measured at 120 K with f s of 10, 30, 100, 300 and 1000 Hz, which corresponded to respective z_0 s of 3.37, 3.24, 3.10, 2.97 and 2.83 nm. N_{bt} varied little in the depth direction. Nearly no influence of Al-PMA could be observed. Note the maximum z_0 is 3.37 nm, which is slightly greater than the thickness (3.3 nm) of GeO_2 in 425°C-PTO MOSCAPs. However, no sudden change in N_{bt} at $z_0 = 3.37$ nm for 425°C-PTO MOSCAPs was observed. Accordingly, there should be errors in GeO_2 thickness or z_0 .

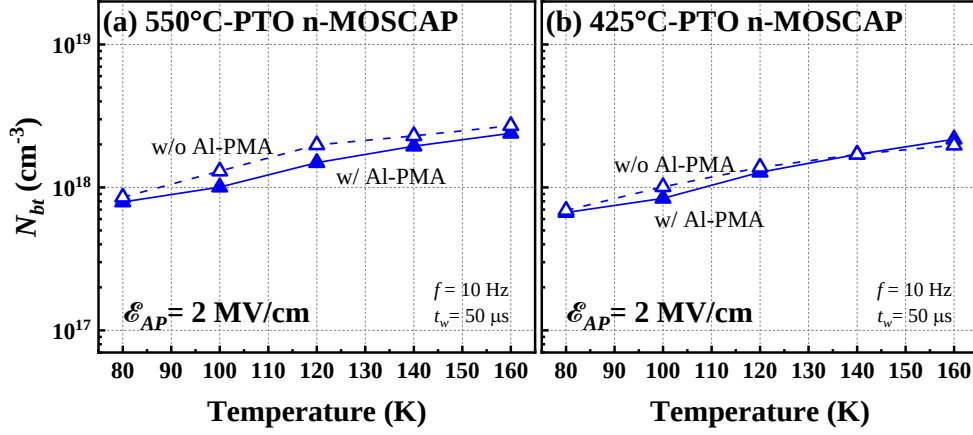


FIG. 3.10 Temperature dependence of N_{bt} for n-MOSCAPs with and without Al-PMA thermally oxidized at (a) 550 °C and (b) 425 °C.

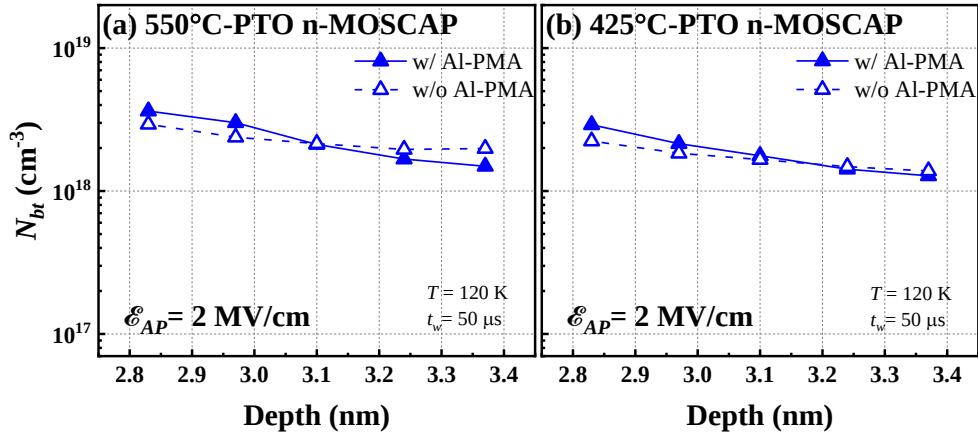


FIG. 3.11 N_{bt} depth profiling for n-MOSCAP with and without Al-PMA thermally oxidized at (a) 550 °C and (b) 425 °C.

Actually, the calculation of z_0 was done by assuming all the BTs exist at a single level with the energy same as Ge band edge. However, BTs can exist in a wide range of energy level. Therefore, the error of z_0 must be estimated. In this study, the depth distribution of BTs was measured at 120 K with pulse frequencies in the range of 10 – 1000 Hz and a pulse intensity E_{AP} of 2 MV/cm (corresponding to an electrical field intensity of 1.37 MV/cm in GeO_2 layer). The

maximum z_0 was obtained by setting pulse frequency to 10 Hz. As for n-MOSCAPs, by using the model in Section 2.3.2, considering all the BTs has the same energy as the conduction band edge of Ge, and neglecting the band bending of GeO_2 during capture and emission, namely the tunneling barrier heights for all the BTs are 1.6 eV (the conduction band offset between GeO_2 and Ge), then the maximum depth of measured BTs is 3.37 nm. At this depth, however, the 0.46 eV band bending induced by the electrical field ($1.37 \text{ MV/cm} \times 3.37 \text{ nm} = 0.46 \text{ V}$) is not negligible. The band diagram during pulse period is illustrated in Fig. 3.12. If there is a wide energetical distribution of BTs, the BTs with energy higher than (up to 0.46 eV) Ge conduction band edge can also capture electrons through tunneling. During the emission process, the barrier height of tunneling for electrons captured by these BTs can be as low as 1.14 eV ($1.6 - 0.46 = 1.14 \text{ eV}$). Because Fermi level was tuned to the midgap during emission, in principle, all the BTs in the energy range from the midgap to the energy 0.46 eV higher than Ge conduction band edge can emit electrons. In the case of BTs located in the energy range from the midgap to Ge conduction band edge, they emit electrons via a cascade emission assisted by ITs, namely tunneling from BTs to ITs and then thermally emitting from ITs to Ge conduction band. At 120 K, DLTS cannot detect ITs with energy lower than a certain deep level (0.23 eV below Ge conduction band edge), due to their too-slow emission process. As the result, considering the cascade emission mechanism, BTs with energy 0.23 eV below Ge conduction band edge also cannot be detected by DLTS no matter how fast the tunneling process is. Then, we can judge the maximum tunneling barrier height is 1.83 eV ($1.6 + 0.23 = 1.83$) for all the BTs detected by DLTS. Now we can consider two extreme conditions that all the BTs locate at a single level having tunneling barrier heights of 1.14 and 1.83 eV, respectively. For these two conditions, we can precisely calculate the respective depth of BTs. The results are 3.99 and 3.15 nm. Because the actual energetical distribution of BTs is always an intermediate condition between these two extreme conditions, the maximum error of depth

evaluation should be approximately 18%. Note the model used in Section 2.3.2 gives a result of 3.37 nm. Similarly, we can also estimate this error for p-MOSCAPs with a result of 5%, which is much smaller than that of n-MOSCAPs owing to the larger valence band offset between GeO_2 and Ge.

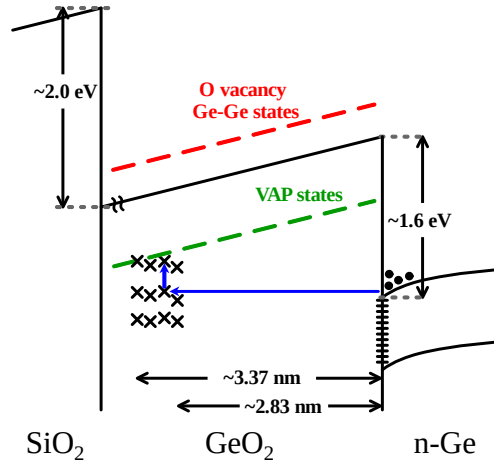


FIG. 3.12 Schematic of detected BTs and ITs in a band diagram of n-MOSCAP. BTs are distributed in a few energy levels near to the conduction band.

Figure 3.12 demonstrates the distribution of IT and BT measured from an n-MOSCAP. As discussed before, the 2 MV/cm $\mathcal{E}_{AP}$ corresponded to an electrical field intensity of 1.37 MV/cm in GeO_2 layer, induced a band bending of approximately 0.4 eV at the depth (from the GeO_2/Ge interface) of around 3 nm. This meant the electrons tunneled to the BTs located at an energy position higher (0.4 eV) than the conduction band edge of Ge. It is believed that there were some BTs located near to this energy position and all the BTs were distributed in a certain energy range. Therefore, the tunneled electrons could be emitted to other BTs within this energy range. This was why we could observe the temperature dependence of N_{bt} in Fig. 3.10. It has been found that an oxygen-related vacancy can be generated during thermal oxidation [19]. However, the energy states of the oxygen vacancy are located in the conduction band of GeO_2 and relatively far from

the conduction band of Ge, so the carrier trapping problem is less serious. Another possible physical origin is the valence alternation pair (VAP), whose energy states are less than 1 eV above the Ge conduction band edge [20], which is consistent with the band diagram shown in Fig. 3.12. Even though the N_{bt} value in n-MOSCAPs is not especially high, the low tunneling barrier allows the capture/emission process more aggressive, resulting in a higher value of I_{DLTS} in n-MOSCAPs compared with p-MOSCAPs (Fig. 3.4 and 3.5).

3.6 N_{bt} of MOSCAPs fabricated by ECR plasma oxidation

Figure 3.13 shows the temperature dependence of N_{bt} for MOSCAPs fabricated by ECR plasma oxidation. There was nearly no temperature dependence of N_{bt} in p-MOSCAPs, which indicated that no thermal emission process was involved in the N_{bt} measurement. N_{bt} of p-MOSCAP without Al-PMA was apparently high compared with those of PTO samples as shown in Fig. 3.8. Even after Al-PMA, the N_{bt} values were still higher than those of the PTO p-MOSCAPs, which implied the relatively poor quality of the GeO_2 layer fabricated by ECR plasma oxidation. As discussed previously, this may have resulted from the rather low fabrication temperature of ECR. Furthermore, the mechanism of the plasma oxidation should be different from that of thermal oxidation, and more traps might be precipitated in the plasma oxidized GeO_2 . In the case of the n-MOSCAPs without Al-PMA, N_{bt} was lower than that of the PTO n-MOSCAPs. This was reasonable because the measured BT position was located in the SiO_2 layer, which contained much less BTs than GeO_2 . In addition, N_{bt} in SiO_2 was increased by Al-PMA, which was different from the case of GeO_2 , implying a different nature of the BTs between SiO_2 and GeO_2 .

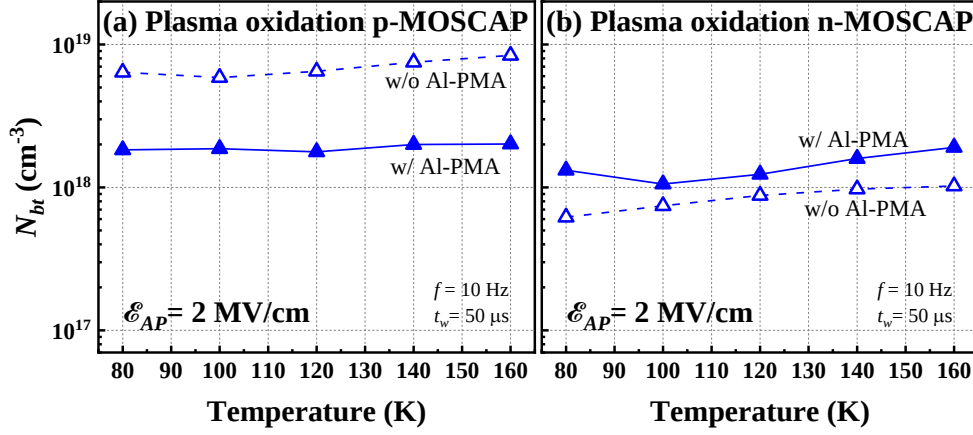


FIG. 3.13 Temperature dependence of N_{bt} for plasma oxidized (a) p-MOSCAPs and (b) n-MOSCAPs.

3.7 Summary of this chapter

N_{bt} of GeO_2/Ge gate stacks was successfully evaluated by using DLTS. DLTS signals were decomposed into IT signals and BT signals according to their features. D_{it} and N_{bt} of several MOSCAPs fabricated by thermal oxidation and ECR plasma oxidation were investigated. BTs at the position of 0.4 nm from the GeO_2/Ge interface were measured for p-MOSCAPs. In the case of n-MOSCAPs, BTs at the position range of 2.8 to 3.4 nm from the GeO_2/Ge interface were measured and N_{bt} varied little in the depth direction. N_{bt} values of both p- and n-MOSCAPs are in the same range ($\sim 10^{18} \text{ cm}^{-3}$). The energy level of BTs near to the valence band edge should be centralized in a narrow range, while those near to the conduction band edge should be distributed over a relatively wide range. The influences of the processing temperatures, oxidation methods, and Al-PMA on the quality of the gate stacks were clearly observed. A higher processing temperature is beneficial to lower D_{it} s and N_{bt} s, namely to increase the quality of the gate stacks. Al-PMA can passivate ITs and BTs near to the valence band edge of Ge but not those near to the conduction band edge. Even though the N_{bt} value in n-MOSCAPs is not especially high, the low

tunneling barrier allows the capture/emission process more aggressive. Since the N_{bt} value of n-MOSCAP might originate from the VAP state with an energy close to 1 eV above the conduction band edge of Ge, passivation or elimination of these states are essential to realize high channel-mobility for n-MOSFETs.

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Chapter 4 Interface trap and border trap characterization for $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ gate stacks and influence of these traps on mobility of Ge p-MOSFET [1]

4.1 Introduction

In chapter 3, a newly-developed BT evaluation method using DLTS has been successfully applied to $\text{SiO}_2/\text{GeO}_2/\text{Ge}$ MOSCAPs fabricated by thermal oxidation and plasma oxidation. When we consider the application of Ge for scaled CMOS devices, it is necessary to introduce high- k gate stack with good interface quality and thin EOT. One candidate, $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ gate stack, has been suggested by Takagi *et al.* [2–5]. The gate stack was formed by atomic layer deposition (ALD) of Al_2O_3 and subsequent ECR post plasma oxidation (PPO). They successfully achieved thin EOT (<1 nm), low D_{it} ($\sim 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$), and effective electron and hole mobilities of Ge MOSFETs higher than Si universal mobilities. For better understanding, BT in high- k gate stacks is a great interest. However, BT evaluation for the high- k gate stack on Ge is limited [6]. Besides, although mobility degradation mechanism by scattering factors for Si MOSFETs has been studied deeply, similar study for Ge MOSFETs has not been carried out. In this chapter, inclusive study about IT, BT, fixed charge, surface roughness, and effective hole mobility are performed. In section 4.2, MOSCAP and MOSFET fabrication method are described. In section 4.3, the structural analyses and electrical properties including IT, BT, and fixed charge for $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ gate stacks are investigated. In section 4.4, the electrical properties of Ge p-MOSFETs with the same gate stacks are evaluated. The effect of surface roughness and BTs on the mobility of

MOSFETs are also discussed.

4.2 Sample fabrication

The fabrication process of MOSCAPs is as follows. The p-type (100) Ge substrate with a doping concentration of $2.3 \times 10^{16} \text{ cm}^{-3}$ was used. After chemical cleaning by acetone and a HF solution, the first layer of Al_2O_3 was deposited at 300°C by ALD with precursors of water and trimethylaluminum for 3, 9, 14 and 20 cycles, corresponding to four samples, followed by PPO using ECR at room temperature with a microwave power of 500 W and Ar/O_2 flow rates of 18/3 sccm for 1 min. The second layer of Al_2O_3 was deposited at 300°C by ALD for 25 cycles to avoid current leakage during electrical measurements. For comparison, one sample with 45 cycles of Al_2O_3 deposition by ALD without PPO was also fabricated. 400°C PDA was performed for 30 min. Then, the TiN layer as a gate electrode was deposited by sputtering, followed by 350°C PMA

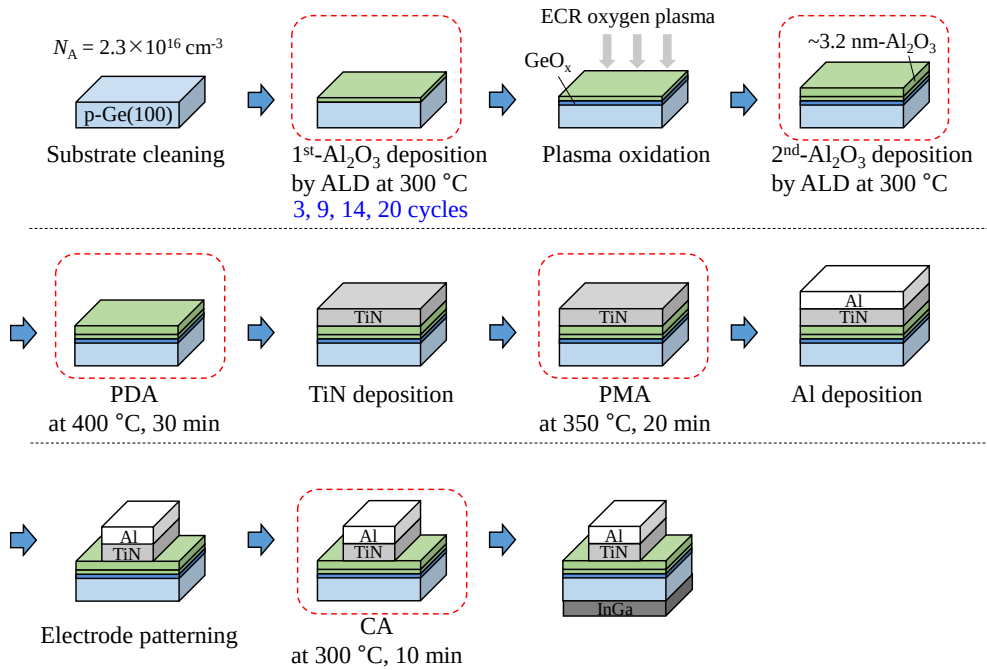


FIG. 4.1 Fabrication process of Al/TiN/Al₂O₃/GeO_x/p-Ge MOSCAPs.

for 20 min. After that, the Al layer was also deposited and the gate electrode was patterned by lithography and wet etching. Here, the H_3PO_4 -based acid and the $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2$ solution were used for Al and TiN etching, respectively [7]. To improve the electrical contact between TiN and Al layers, contact annealing (CA) was performed at 300°C for 10 min. Finally, an InGa back contact was formed. All annealing in this study was performed in N_2 ambient. The fabrication process is shown in Fig. 4.1.

Ge p-MOSFETs were fabricated on an n-type (100) Ge substrate with a doping concentration of $9.3 \times 10^{15} \text{ cm}^{-3}$. A gate-first process was carried out. The process flow is shown in Fig. 4.2. After wafer cleaning, SiO_2 field oxide was deposited by ECR sputtering for isolation. Then, windows were opened by standard lithography and wet etching to define the active areas. To eliminate the influences of sputtering and etching on the surface of the active area, sacrificial GeO_2 was grown by thermal oxidation at 450°C for 30 min in O_2 ambient and removed by rinsing in a dilute HF solution. Next, an $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ gate stack was fabricated by the same method as MOSCAPs as mentioned above. After 400°C PDA, the Al/TiN gate electrode was deposited and patterned. To form S/D, 80 nm- SiO_2 for controlling ion implantation depth was deposited by ECR plasma sputtering with a lift-off method, and the B ion implantation was carried out with an acceleration energy of 30 keV and a dose of 10^{15} cm^{-2} , which was calculated from the simulation result of the stopping and range of ions in matter (SRIM) [8]. The Al/Pt contact electrode for S/D was formed by the lift-off method, followed by CA and activation annealing (for S/D) at 300°C for 10 min in N_2 ambient. Pt has high work function of 5.5 eV, allowing formation of ohmic contact on p-Ge with low resistance [9]. Subsequently, an InGa back contact was formed. The parameters for ECR plasma oxidation, ECR SiO_2 deposition, TiN and Pt deposition are listed in Table 4.1 and 4.2. The active hole density of $4.3 \times 10^{19} \text{ cm}^{-3}$ in B implanted S/D region was confirmed by Hall effect measurement. Both D_{it} and N_{bt} were characterized using DLTS, and the

pulse frequency of 10 Hz was set (see section 2.3) [10–12].

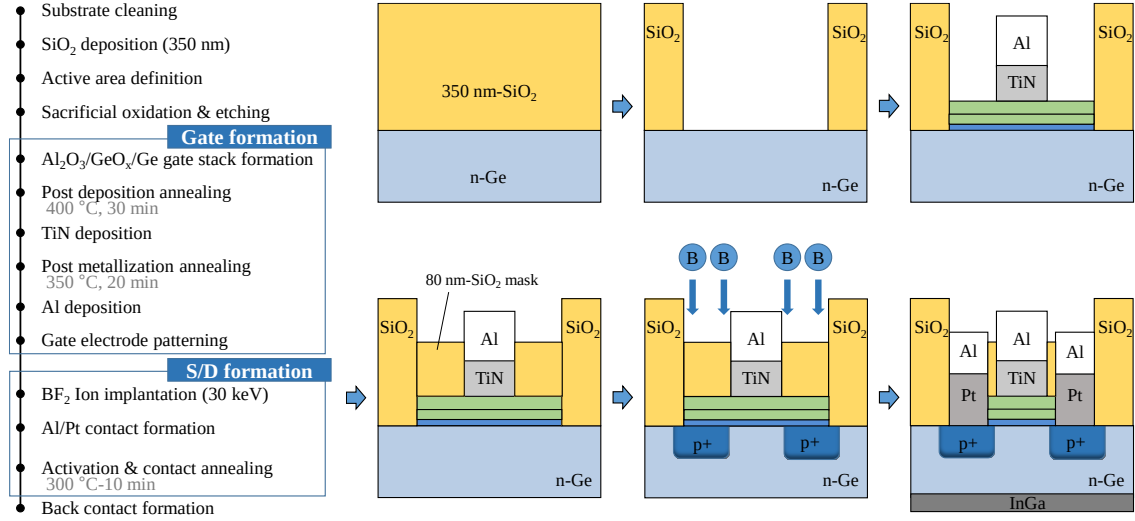


FIG. 4.2 Fabrication process of Ge p-MOSFETs with $\text{Al}_2\text{O}_3/\text{GeO}_x$ gate stacks.

TABLE 4.1 Parameters for ECR plasma oxidation and SiO_2 deposition.

Parameter	Plasma oxidation for		SiO_2 deposition for	
	isolation	gate formation	isolation	B implantation
Microwave power: P_μ (W)	300	500	500	500
rf Power: P_{rf} (W)	0	0	500	500
Ar flow rate (sccm)	30	18	16	16
O_2 flow rate (sccm)	0.1	3	8	8
Pressure (Pa)	0.22	0.15	0.15	0.15
Deposition rate (nm/min)	--	--	3.1	3.1
Temperature ($^\circ\text{C}$)	130	RT	130	RT
Time	3 min	1 min	116 min 40 sec	25 min 48 sec

TABLE 4.2 Sputtering parameters for TiN and Pt deposition.

Parameter	TiN	Pt
rf power: P_{rf} (W)	60	10
Ar flow rate (sccm)	30	20
Pressure (Pa)	2	4
Deposition rate (nm/min)	5.0	3.3
Temperature (°C)	RT	RT
Time	5 min	7 min 35 sec

4.3 Structural analyses and electrical properties for $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ gate stacks

To clarify the formation of the GeO_x interlayer, XPS measurement was carried out. Figure 4.3 shows the Ge 3d XPS spectra of Ge gate stacks with and without PPO at a photoelectron take-off angle of 90°. A monochromatic Al K- α X-ray source was used. The spectra were calibrated with a Ge 3d core level (29.3 eV) and normalized by the signal intensity of Ge bulk. The Ge oxide signal intensity decreases with increasing cycle number of the first Al_2O_3 layer. Simultaneously, the Ge oxide peak shifts to the low-energy direction, indicating that there is a change in the stoichiometry of Ge and oxygen. In other words, the x in GeO_x becomes less than 2 with decreasing energy of the Ge oxide peak (the lower the energy, the smaller the x in GeO_x). The spectrum of the 20-cycle one is well overlapped with that of the one without oxidation.

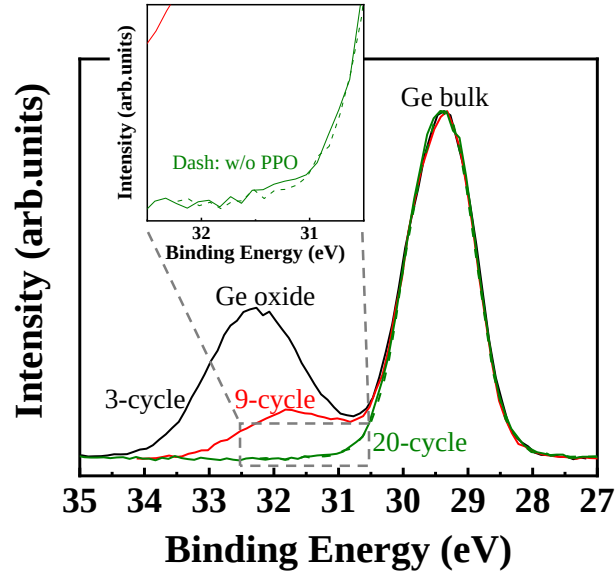


FIG. 4.3 Normalized Ge 3d XPS spectra for $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ structures with and without PPO.

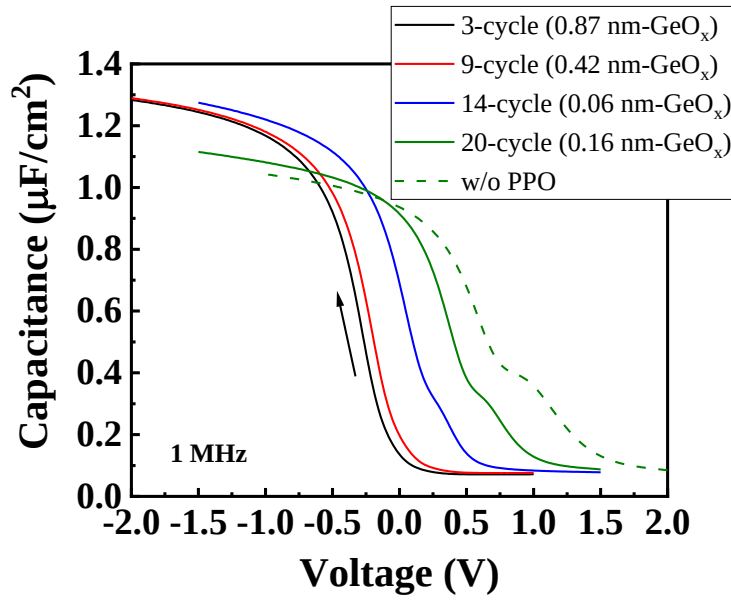


FIG. 4.4 C-V characteristics of $\text{Al}/\text{TiN}/\text{Al}_2\text{O}_3/\text{GeO}_x/\text{p-Ge}$ MOSCAPs with different cycle number of first- Al_2O_3 . The measurement was performed at RT with a frequency of 1 MHz.

The electrical properties of $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ gate stacks were examined by using MOSCAPs. Figure 4.4 shows the C - V curves of $\text{Al}/\text{TiN}/\text{Al}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ MOSCAPs with varied cycle numbers of the first Al_2O_3 layer deposition. With increasing cycle number, the V_{FB} shifts to the positive direction, and a bit stretch-out and small bumps can be seen. However, for the MOSCAP without PPO, V_{FB} is even more positive, and the bump is bigger than the others. Even though the Ge oxide signal was not detected by XPS (Fig. 4.3) for the 20-cycle one, the difference in C - V curves (Fig. 4.4) of 20-cycle and w/o PPO can be seen. Therefore, we believed that there is a Ge oxide layer in the 20-cycle one, or at least the interface property was changed during PPO. A similar clue can be found in the D_{it} result, and will be discussed in a later part. The thickness and EOT for each oxide layer is listed in Table 4.3. Here, Al_2O_3 thickness was measured by ellipsometry. To calculate the EOT of each dielectric layer, permittivities of Al_2O_3 and GeO_x were assumed to be 8.47 and 5.7, respectively. With increasing cycle number of the first Al_2O_3 layer, the GeO_x layer becomes thinner.

TABLE 4.3 Thickness and EOT of each dielectric layer for $\text{Al}/\text{TiN}/\text{Al}_2\text{O}_3/\text{GeO}_x/\text{p-Ge}$ MOSCAPs with different cycle numbers of first- Al_2O_3 . Al_2O_3 thickness was measured by ellipsometry, and the permittivities of Al_2O_3 and GeO_x were assumed to be 8.47 and 5.7, respectively.

1st- Al_2O_3 cycle number	1st- Al_2O_3 thickness (nm)	2nd- Al_2O_3 thickness (nm)	1st + 2nd Al_2O_3 EOT (nm)	MOS EOT (nm)	GeO_x EOT (nm) (MOS EOT- Al_2O_3 EOT)	GeO_x thickness (nm)
3-cycle	1.02	3.2	1.94	2.54	0.60	0.87
9-cycle	1.65	3.2	2.23	2.52	0.29	0.42
14-cycle	2.14	3.2	2.46	2.5	0.04	0.06
20-cycle	2.73	3.2	2.73	2.84	0.11	0.16

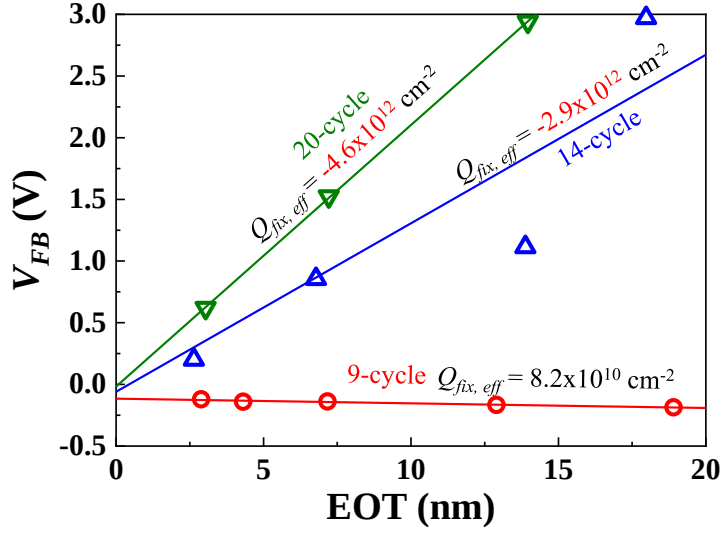


FIG. 4.5 V_{FB} -EOT plots for Ge MOSCAPs with different cycle numbers of first- Al_2O_3 .

The V_{FB} shift is found in Fig. 4.4 even though the EOTs for all MOSCAPs are nearly the same. This is considered as an effect of fixed charges in first Al_2O_3 or GeO_x . To clarify the density of fixed charges ($Q_{fix,eff}$), another set of MOSCAPs with varied cycles of second Al_2O_3 deposition were fabricated while the cycle numbers of first Al_2O_3 deposition were fixed. Their V_{FB} s are plotted in Fig. 4.5. Since V_{FB} s are linearly dependent on the EOT while the cycle numbers of first Al_2O_3 deposition were fixed, the second Al_2O_3 is free of volume charges within the detection limit [13]. V_{FB} is given by the following expression:

$$V_{FB} = \Phi_{MS} - \frac{qQ_{fix,eff}}{\epsilon_{\text{SiO}_2}\epsilon_0} EOT, \quad (4.1)$$

where Φ_{MS} is the work function difference between the metal gate electrode and semiconductor, ϵ_{SiO_2} is the dielectric constant of SiO_2 and ϵ_0 is the permittivity in vacuum. Since the electrode material and substrate doping were not changed, $Q_{fix,eff}$ can be derived from the slope of plots

without the information of Φ_{MS} . The fitting of data with Eq. (4.1) revealed positive $Q_{fix,eff}$ with a density of $8.2 \times 10^{10} \text{ cm}^{-2}$ in the 9-cycle capacitor and negative $Q_{fix,eff}$ with densities of $2.9 \times 10^{12} \text{ cm}^{-2}$ and $4.6 \times 10^{12} \text{ cm}^{-2}$ in the 14- and 20-cycle capacitors, respectively. It was reported that ALD-grown Al_2O_3 contributes the negative polarity of interface fixed charges [14–16], while GeO_2 contributes the positive fixed charges [17–19]. Therefore, the $Q_{fix,eff}$ became more and more positive with decreasing cycle number of the first Al_2O_3 , due to thicker GeO_x . Accordingly, the V_{FB} shifted negatively when the GeO_x layer was formed, which coincides with the finding of Matsuoka *et al* [16].

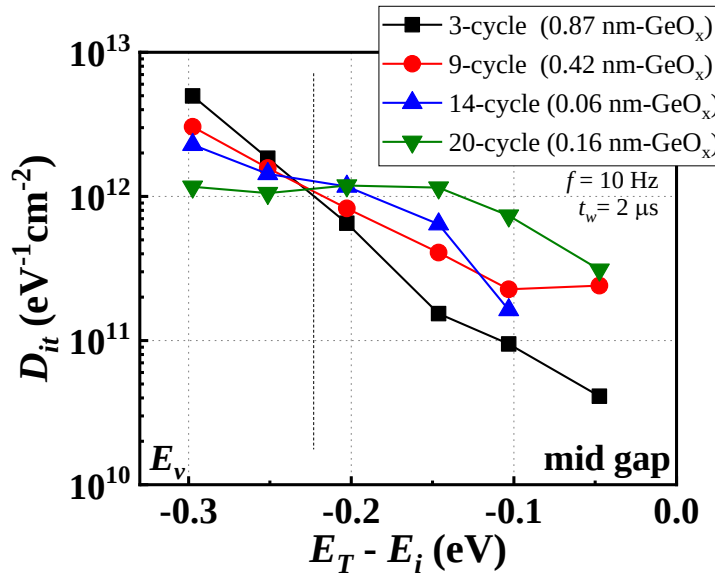


FIG. 4.6 Energy distribution of D_{it} for Al/TiN/ Al_2O_3 / GeO_x /p-Ge MOSCAPs with different cycle numbers of first- Al_2O_3 .

Figure 4.6 shows the energy distribution of D_{it} . In the region close to the midgap, a lower D_{it} can be achieved by the thicker GeO_x layer. However, in the region close to the valence band, the

thicker GeO_x gives higher D_{it} . It is plausible that the thinner GeO_x interlayer causes a higher D_{it} near the midgap. Many groups have reported similar findings [20–22]. According to the XPS result (Fig. 4.3), when the GeO_x interlayer is thinner, GeO_x is composed of a higher portion of suboxides due to the shift of the Ge oxide peak. This could imply an increase in imperfect Ge-O or Ge-Ge bonds at the interface, causing the increase in D_{it} . By contrast, the D_{it} near the valence band decreases with decreasing GeO_x thickness. This phenomenon is similar to the defect termination during Al post-metallization annealing reported previously [23]. The thinner the GeO_x interlayer, the higher the chance of Al oxide existence at the interface, thus decreasing the D_{it} near the valence band. Because the 20-cycle sample contains an ultrathin GeO_x interlayer, Al_2O_3 possibly exists at the GeO_x/Ge interface. Instead, to be more precise, the interface could be considered as a mixture of Al oxide and GeO_x , and this Al-bonded oxide acts as the defect terminator as found in the previous work [23].

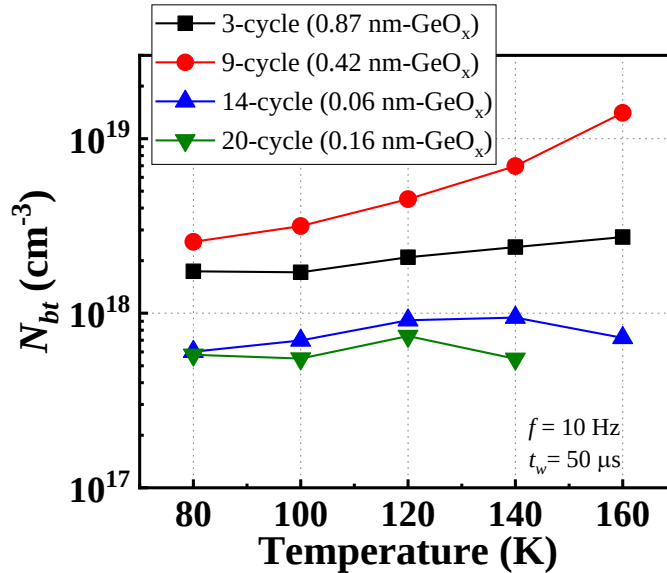


FIG. 4.7 Temperature dependence of N_{bt} for Al/TiN/ Al_2O_3 / GeO_x /p-Ge MOSCAPs with different cycle numbers of first- Al_2O_3 .

Figure 4.7 shows the N_{bt} for all capacitors. The details of the measurement have been shown in section 2.3.2 [10–12]. The highest and lowest N_{bt} were observed in the 9- and 20-cycle capacitors, respectively. The temperature dependence of N_{bt} is obvious for the 9-cycle capacitor. Based on our measuring condition of N_{bt} , detected BT signals originated from the position with a depth of 0.4 nm measured from the GeO_2/Ge interface when the tunneling barrier is the valence band offset (~ 3.6 eV) at the interface [10,24]. According to the thickness of GeO_x in Table 4.3, the detected BT position can be categorized into three cases, as shown in Fig. 4.8. Since the GeO_x thickness of the 3-cycle capacitor is over 0.4 nm, the detected BT signals are from GeO_x (Fig. 4.8 (a)). The GeO_x thickness of the 9-cycle capacitor is approximately 0.4 nm, implying that the detected BT signals are from the $\text{Al}_2\text{O}_3/\text{GeO}_x$ interface region (Fig. 4.8 (b)). The GeO_x thickness of 14-cycle and 20-cycle capacitors is less than 0.4 nm, indicating that the detected BT signals are from Al_2O_3 (Fig. 4.8 (c)). Here, the actual position of the detected BTs should be less than 0.4 nm when we consider the valence band offset (~ 5.4 eV for $\text{Al}_2\text{O}_3/\text{Ge}$) of $\text{Al}_2\text{O}_3/\text{GeO}_x$ [25]. Even if we take into account the GeO_x stoichiometry change, which may slightly reduce the band offset of GeO_x/Ge , the measuring position should be still in Al_2O_3 . After matching the BT position with N_{bt} , N_{bt} in GeO_x ($\sim 2 \times 10^{18} \text{ cm}^{-3}$) is higher than that in Al_2O_3 ($6\text{--}9 \times 10^{17} \text{ cm}^{-3}$), and the highest N_{bt} is in the $\text{Al}_2\text{O}_3/\text{GeO}_x$ interface region ($\sim 1 \times 10^{19} \text{ cm}^{-3}$). The temperature dependence found in N_{bt} of the 9-cycle capacitor implies the thermal process involved, and this is another clue that the signals are from the interface.

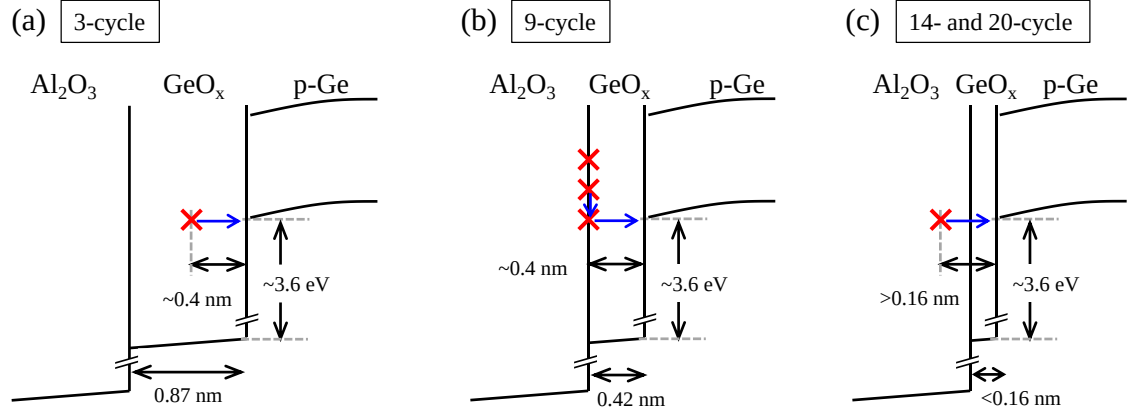


FIG. 4.8 Origin of detected BT signals of Al/TiN/Al₂O₃/GeO_x/p-Ge MOSCAPs with first-Al₂O₃ deposition for (a) 3-cycle, (b) 9-cycle and (c) 14- and 20-cycle.

4.4 Ge p-MOSFETs with Al₂O₃/GeO_x/Ge gate stacks

Figure 4.9 shows I_D vs drain voltage (V_D) characteristics of p-MOSFETs with the Al₂O₃/GeO_x/Ge gate stack. Here, the L and width W are 120 μm and 390 μm , respectively. The p-MOSFETs with a higher cycle number of the first Al₂O₃ layer showed higher current drivability. Figure 4.10 shows I_D and source current (I_S) vs V_G characteristics with $V_D = -10$ mV. High off-states I_{DS} at positive V_{GS} are caused by the drain/substrate leakage current [26,27]. Here V_{TH} was obtained from the x-axis interception of $I_S / g_m^{1/2}$ vs V_G plots [28], where g_m is the transconductance, and V_{TH} for each sample are indicated as solid circles in Fig. 4.10. V_{TH} shifts to the positive direction with increasing cycle number, which is consistent with the V_{FB} shift obtained in $C-V$ characteristics.

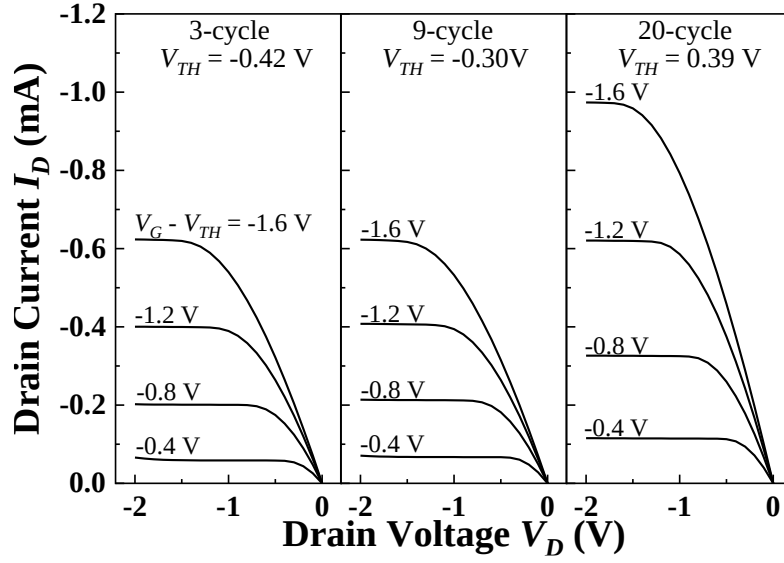


FIG. 4.9 I_D - V_D characteristics of Ge p-MOSFETs with different cycle numbers of first- Al_2O_3 . All the devices have $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ gate stacks with the same fabrication process as the MOSCAPs. The L and W were $120\text{ }\mu\text{m}$ and $390\text{ }\mu\text{m}$, respectively.

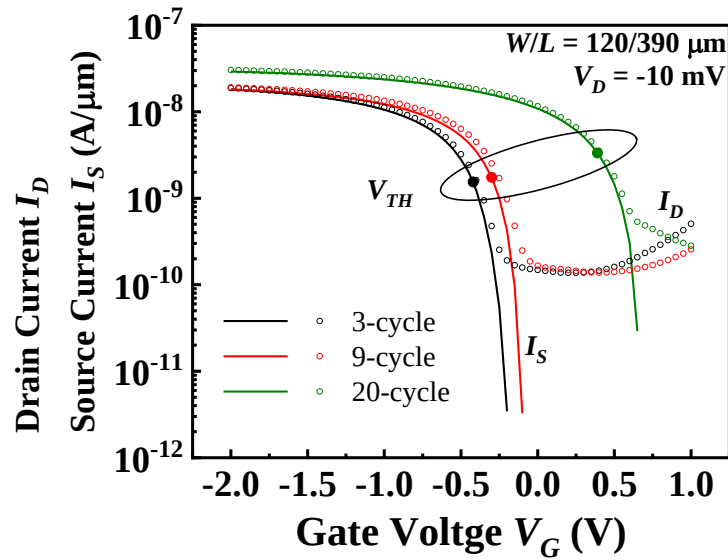


FIG. 4.10 I_D - and I_S - V_G characteristics of Ge p-MOSFETs with different cycle numbers of first- Al_2O_3 .

Figure 4.11 shows the mobility of p-MOSFETs calculated by the split *C-V* method [29]. All p-MOSFETs showed similar peak mobility (170-200 cm²/Vs) at a low inversion carrier density region. On the other hand, in the high inversion carrier density region, the mobility of the 20-cycle one is higher than that of the others. In the case of Si MOSFET, the mobility degradation in the high-field region is usually considered as an effect of surface roughness scattering [30]. In this paper, a potential cause for the difference in surface roughness is the plasma oxidation process. In principle, plasma oxidation should have the greatest impact on the 3-cycle sample and an almost negligible impact on the 20-cycle sample by considering the different thicknesses of the first-Al₂O₃ layer and the formed GeO_x layer. In addition, since the 3-cycle sample shows lower mobility than the 20-cycle one in the high-field region, the 3-cycle sample is supposed to have a rougher interface of GeO_x/Ge. To confirm this, scanning transmission electron microscopy (STEM) analysis was performed. Figure 4.12 shows a STEM high-angle annular dark-field (HAADF) image of the Al/TiN/Al₂O₃/GeO_x/Ge gate stack with 3-cycle first-Al₂O₃ deposition. The root mean square (rms) roughness value of the interface of GeO_x/Ge is approximately 0.2 nm, which is nearly the same level as a commercial Ge wafer surface (0.19 nm) measured by using an atomic force microscope (AFM), implying that the surface roughness may not be the factor of the mobility degradation in the high-field region. To reconfirm the interface roughness, the oxide layers were removed by using 0.5% HF solution and measured the surface roughness of two extreme cases, 3-cycle and 20-cycle, by using an AFM [31].

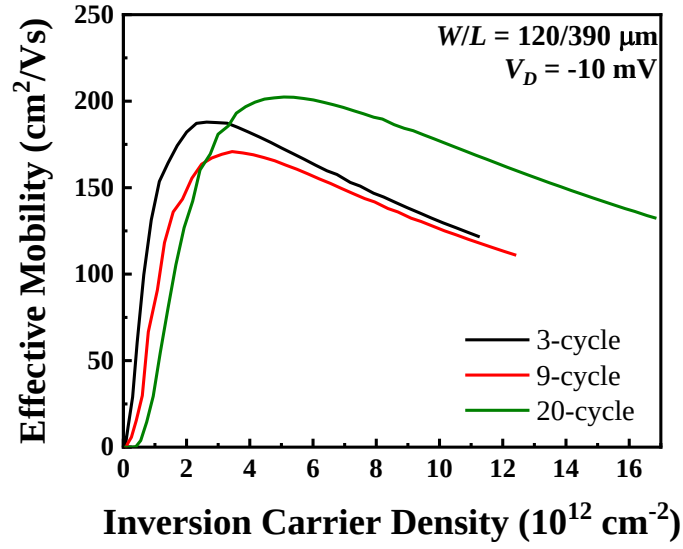


FIG. 4.11 Effective hole mobility in Ge p-MOSFETs with different cycle numbers of first- Al_2O_3 .

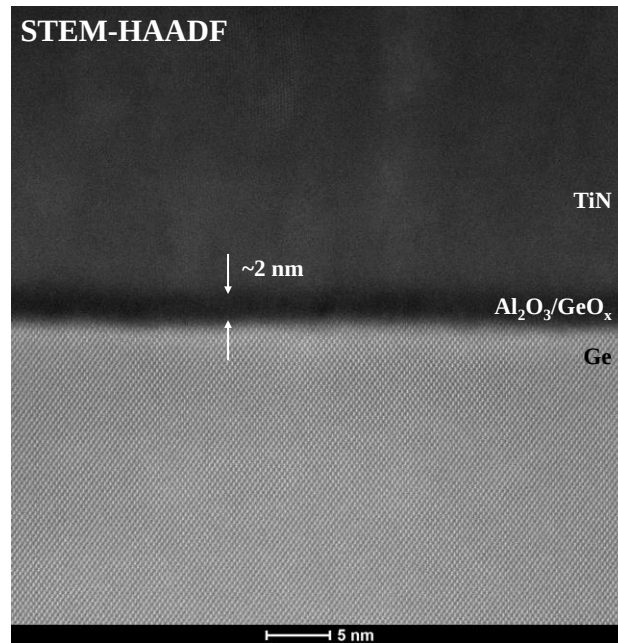


FIG. 4.12 A STEM-HAADF image of $\text{Al}/\text{TiN}/\text{Al}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ gate stacks with 3-cycle first- Al_2O_3 deposition and without second- Al_2O_3 deposition.

Figure 4.13 shows $1 \times 1 \mu\text{m}^2$ AFM images of the GeO_x/Ge interface. The rms roughness values of 3- and 20-cycle samples are 0.21 nm and 0.20 nm, respectively, which are entirely consistent with the STEM result. Since the formation of native oxide of Ge is layer-by-layer growth [32], the morphology of the Ge surface can be copied to the surface of its native oxide. Therefore, there is no doubt that these AFM measurements can provide the information of interface roughness. Consequently, the effect of surface roughness scattering cannot explain the mobility degradation in the high-field region.

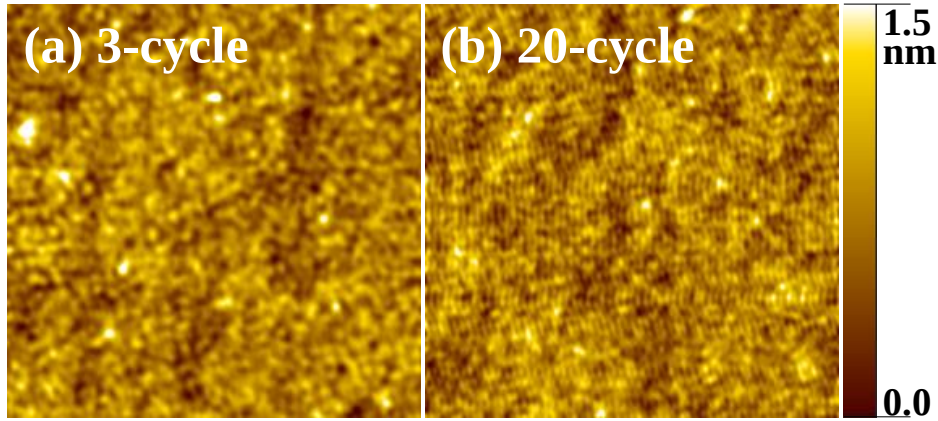


FIG. 4.13 AFM image of GeO_x/Ge interface for the $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ structure with first- Al_2O_3 deposition for (a) 3-cycle and (b) 20-cycle. The $\text{Al}_2\text{O}_3/\text{GeO}_x$ was removed by dilute HF, and the AFM measurements were performed in $1 \times 1 \mu\text{m}^2$.

Instead of surface roughness, BTs may be a relatively reasonable factor in this case. To discuss the connection between BTs and effective mobility, the band bending and trap states at different MOSFET operating conditions were considered. Figure 4.14 shows the band diagrams of $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ gate stacks at room temperature under weak inversion ($\phi_s = \Psi_B$), strong inversion (approximately $\phi_s = \Psi_B + 0.23 \text{ eV}$ in this case), and even stronger inversion ($\phi_s > \Psi_B + 0.5 E_g$),

where ϕ_s is the surface potential. It is worth noting that the charge neutrality level is ~ 0.23 eV under the E_i of Ge [33]. Under weak inversion (Fig. 4.14 (a)), the acceptor-like ITs near the lower half of the bandgap showing negative charges cause mobility degradation. Under strong inversion (Fig. 4.14 (b)), there is nearly no contribution of neutral charged ITs to mobility degradation. When the inversion gets even stronger (Fig. 4.14 (c)), the donor-like ITs near the valence band showing positive charges cause mobility degradation. Besides, the BTs have a higher chance to capture holes (carriers) at this state due to the high electric field. Therefore, both ITs and BTs near the valence band cause mobility degradation in the high-field region. A similar finding about the effect of traps in the insulating oxide near the interface on mobility degradation in the high-field region was reported in a Si-based memory device study, even though the traps were not called BTs there [34].

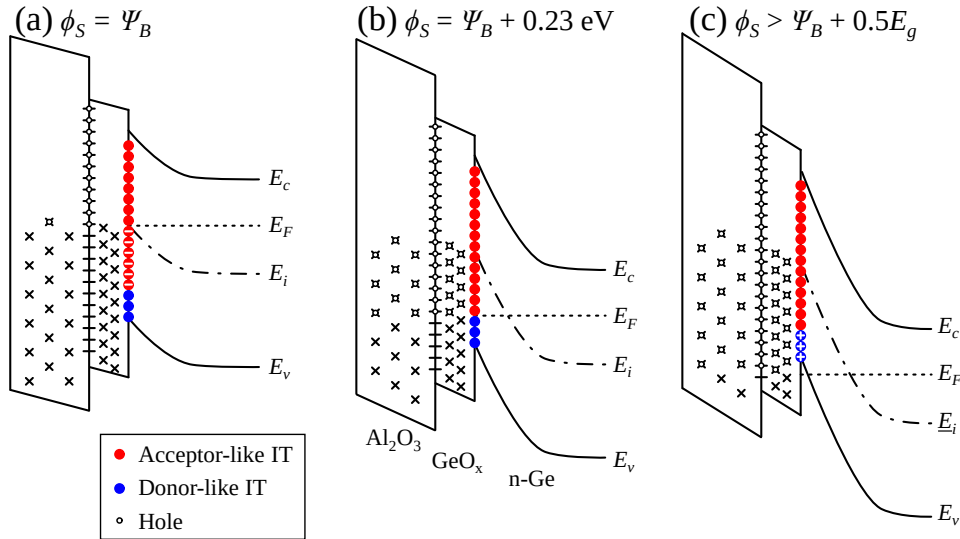


FIG. 4.14 Band diagrams of a Ge p-MOSFET showing the occupancy of ITs and BTs when (a) $\phi_s = \Psi_B$, (b) $\phi_s = \Psi_B + 0.23$ eV and (c) $\phi_s > \Psi_B + 0.5 E_g$ (corresponding to the high-field region). IT net charges are negative at condition (a), neutral at condition (b), and positive at condition (c).

The total effect of BTs in all Ge p-MOSFETs with $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ gate stacks is categorized into two and summarized in Fig. 4.15. Since N_{bt} in Al_2O_3 is smaller than that in GeO_x or at the $\text{Al}_2\text{O}_3/\text{GeO}_x$ interface, the 20-cycle gate with nearly no GeO_x contains fewer BTs in total compared to a 3 or 9-cycle gate. In addition, the 20-cycle gate shows the lowest D_{it} near the valence band, as shown in Fig. 4.6. Thus, in the high-field region, the highest effective mobility was achieved from MOSFETs with 20-cycle first Al_2O_3 . Due to the low N_{bt} near the Ge valence band edge and the defect termination of the GeO_x/Ge interface, Al_2O_3 is an exceptional material for the gate dielectric of Ge p-MOSFETs.

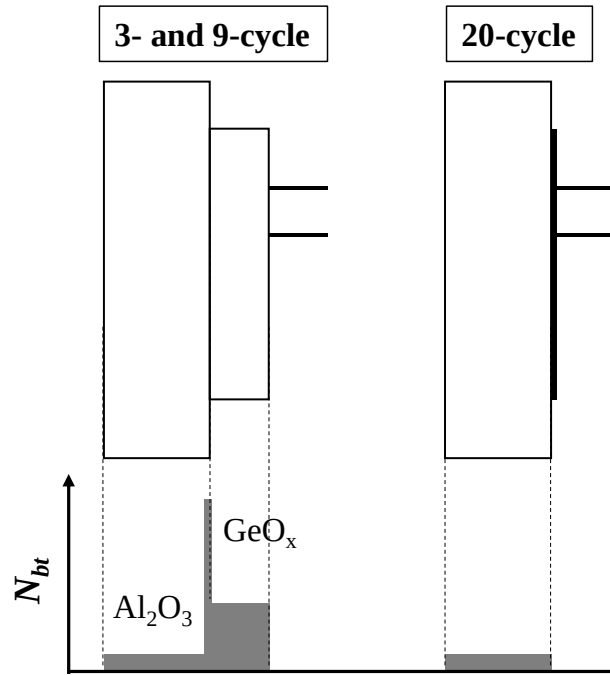


FIG. 4.15 Illustration of N_{bt} in Ge p-MOSFETs with $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ gate stacks.

4.5 Summary of this chapter

By using DLTS, D_{it} and N_{bt} of $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{p-Ge}$ gate stacks with different GeO_x thicknesses fabricated by PPO were evaluated. By changing the thickness of GeO_x , N_{bt} s in the GeO_x interlayer, the $\text{Al}_2\text{O}_3/\text{GeO}_x$ interface region, and the Al_2O_3 layer, respectively, were successfully measured. D_{it} near the midgap is lower in the MOSCAPs with a thicker GeO_x layer. By contrast, D_{it} near the valence band is lower in the MOSCAPs with a thinner GeO_x layer, owing to the defect termination by Al oxide. BTs are mainly located at the $\text{Al}_2\text{O}_3/\text{GeO}_x$ interface region. ITs and BTs near the valence band edge of Ge affect the effective mobility of Ge p-MOSFETs in the high-field region. Therefore, reduction of ITs and BTs near to valence band is the key to reach high-performance p-MOSFETs. In this sense, Al_2O_3 is a suitable dielectric material for Ge p-MOSFETs.

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Chapter 5 Conclusion and outlook

5.1 summary of this study

To realize the high mobility Ge MOSFET, the high-quality Ge gate stacks is necessary. In this study, defect characterization of Ge gate stacks using DLTS was studied for a clear understanding of the influence of defect upon the device performance in order to further improve Ge MOSFET. Since a GeO_x interlayer is effective for D_{it} reduction, the gate stacks with a GeO_x interlayer were characterized. The main conclusions of this thesis are as follows:

1. DLTS analysis for D_{it} and N_{bt} in Ge MOSCAP

The principle of DLTS was described, and the calculation details of different traps at different position of MOS structures are shown. Equations of D_{it} and N_{bt} for GeO_2/Ge structure are derived. By adjusting the measurement parameters, such as temperature, pulse strength, pulse frequency and pulse duration, the different information of IT and BT can be observed. For example, we can change the temperature or pulse frequency to obtain the energy distribution of D_{it} . In contrast, pulse frequency gives the depth information of BT, but temperature cannot provide energy level in principle due to the tunneling mechanism. The measuring depths of N_{bt} in n-MOSCAP and in p-MOSCAP are different due to the different band offset and effective mass of carriers. Although DLTS is effective for evaluation of trap density, different kinds of traps direct to different equations based on their nature. Therefore, identification of the source of DLTS signal is significant for an accurate characterization.

2. DLTS study on SiO₂/GeO₂/Ge gate stacks fabricated by thermal oxidation and plasma oxidation

Ge MOSCAPs with SiO₂/GeO₂/Ge gate stacks were fabricated by thermal oxidation and plasma oxidation and characterized by using DLTS. The IT and BT signals were successfully separated based on their different dependences on the intensity of injection pulses. By using p-MOSCAPs, BTs at the position of 0.4 nm from GeO₂/Ge interface were measured, and the energy of these BTs was centralized at the position near to the valence band edge of Ge. By using n-MOSCAPs, BTs at the position range of 2.8–3.4 nm from the GeO₂/Ge interface were measured, of which N_{bt} varied little in the depth direction. The energy of these BTs were distributed in a relatively wide range near to the conduction band edge of Ge. The influences of the processing temperatures, oxidation methods, and Al-PMA on the quality of the gate stacks were clearly observed. A higher processing temperature is beneficial to lower D_{its} and N_{bts} , namely to increase the quality of the gate stacks. We also found that Al post metallization annealing can passivate both ITs and BTs near to the valence band edge of Ge but not those near to the conduction band edge. Even though the N_{bt} values for both p- and n- MOSCAPs were in the same range ($\sim 10^{18}$ cm⁻³), the low tunneling barrier of n-MOSCAP allows the capture/emission process more aggressive. To realize high channel-mobility for n-MOSFETs, passivation or elimination of the traps, which is likely VAP state with energy close to 1 eV above the conduction band edge of Ge, are essential.

3. DLTS study on Al₂O₃/GeO_x/p-Ge gate stacks fabricated by post plasma oxidation

To investigate the BTs in other oxide materials, Al₂O₃/GeO_x/p-Ge gate stacks were characterized by using DLTS. Through evaluating the gate stacks with different GeO_x thickness, the respective BTs in Al₂O₃, Al₂O₃/GeO_x interface region, and GeO_x were detected.

D_{it} near to mid-gap is lower in the MOSCAPs with a thicker GeO_x , while the D_{it} near to the valence band is lower in the MOSCAP with a thinner GeO_x owing to the defect termination by Al oxide. The N_{bt} in Al_2O_3 ($6\sim 9 \times 10^{17} \text{ cm}^{-3}$) is lower than those in GeO_x ($\sim 2 \times 10^{18} \text{ cm}^{-3}$), and the highest N_{bt} ($\sim 1 \times 10^{19} \text{ cm}^{-3}$) was found in $\text{Al}_2\text{O}_3/\text{GeO}_x$ interface region.

4. Study on influence of D_{it} and N_{bt} on performance of Ge p-MOSFETs with $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ gate stacks

To study the influence of ITs and BTs on mobility, Ge p-MOSFETs with $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{p-Ge}$ gate stacks were fabricated and analyzed. The ITs and the BTs near to valence band edge of Ge affect the effective mobility of Ge p-MOSFETs in high-field region. Therefore, passivation or elimination of ITs and BTs near to valence band edge of Ge should be effective for mobility enhancement in high-field region, and Al_2O_3 is a suitable dielectric material for Ge p-MOSFETs.

5.2 Perspectives

In this thesis, both V_P scan and t_w scan were performed on Ge MOSCAPs with a thick GeO_2 layer to characterize the defects in GeO_2 . According to the results, the DLTS signals of n-MOSCAP were much higher than that of p-MOSCAP due to the low barrier height. Therefore, either BT trap reduction or dielectric materials of large band offset with Ge is suggested for high mobility n-MOSFET. The influence of IT and BT on performance of p-MOSFET was studied, and it is expected to find a similar results on n-MOSFET. Besides, the dielectric materials and fabrication method suitable for Ge n-MOSFET should be studied. Potential studies for the future are as follows:

1. SiO₂/GeO₂/n-Ge gate stack with thin GeO₂

Since SiO₂ is an excellent dielectric material with high band offset and low N_{bt} , p-MOSCAP-like V_p scan and t_w scan (slow grow and low intensity of DLTS signals) may be obtained. Through studying this gate stack, the understanding for BT will be strengthened.

2. Y-doped GeO_x/n-Ge gate stack

Y-doped GeO_x/n-Ge gate stack provides not only a low D_{it} but also a small C - V hysteresis, which may result from VAP termination [1]. Therefore, defect characterization of this gate stack may be helpful for optimizing the fabrication conditions.

3. Ge n-MOSFET

Since the influence of IT and BT on Ge p-MOSFET was studied in this thesis, a similar result for Ge n-MOSFET is expected. The Ge n-MOSFET with the gate stack mentioned above may provide high mobility in high-field region.

4. Other substrate materials

For other applications or other devices, the defect characterization is also important. The defect characterization method developed in this thesis should be applicable to other substrate, such as SiGe and GeSn.

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Appendix: lock-in DLTS and DLTS spectrum

In this study, all DLTS measurement were performed using a SEMILAB DLS83D system with a lock-in DLTS. The capacitance meter is a 1 MHz phase sensitive rectifier. Figure A.1 shows how the lock-in integrator processed the transient capacitance [1]. When Pulse voltage train is applied (Fig. A.1 (a)), capacitance transient is obtained (Fig. A.1 (b)). After multiplied with the lock-in function (Fig. A.1 (c)), the exponential decay capacitance transient becomes like Fig A.1 (d). There is a gate-off time $T_p/20$ at the beginning of every half period to let the measuring

circuit recover. The output signal ΔC is the integration of Fig A.1 (d), which is given by

$$\Delta C = \frac{1}{T_p} \left[\int_0^{T_p/2 - (t_w + T_p/20)} C(t) dt + \int_{T_p/2 - (t_w + T_p/20)}^{T_p/2} C(t) dt - \int_{T_p/2}^{T_p - (t_w + T_p/20)} C(t) dt - \int_{T_p - (t_w + T_p/20)}^{T_p} C(t) dt \right], \quad (\text{A.1})$$

In the case of bulk traps in the p-type semiconductor, $C(t)$ is given by

$$C(t) = -\frac{N_T}{2N_A} C(\infty) e^{-e_s t} + C(\infty), \quad (\text{A.2})$$

when $t \geq 0$ and $N_T \ll N_A$. When the capacitance transient is analyzed by lock-in DLTS, ΔC is given by

$$\Delta C = C(t) - C(\infty) = \frac{N_T}{2N_A} C(\infty) \Phi, \quad (\text{A.3})$$

where $\Phi(x)$ is the lock-in function given by

$$\Phi = \frac{1}{T_p} \left[\int_0^{T_p/2 - (t_w + T_p/20)} e^{-(t + T_p/20)/\tau_s} dt + \int_{T_p/2 - (t_w + T_p/20)}^{T_p/2} e^{-(T_p/2 - t_w)/\tau_s} dt - \int_{T_p/2}^{T_p - (t_w + T_p/20)} e^{-(t + T_p/20)/\tau_s} dt - \int_{T_p - (t_w + T_p/20)}^{T_p} e^{-(T_p - t_w)/\tau_s} dt \right]. \quad (\text{A.4})$$

When we define $x = T_p/\tau_s = e_s/f$, the lock-in function $\Phi(x)$ can be written as follows:

$$\Phi(x) = \left[\frac{1}{x} e^{-\frac{x}{20}} - \frac{1}{x} e^{-\left(\frac{x}{2} - \frac{t_w}{\tau_s}\right)} + \left(\frac{t_w}{T_p} + \frac{1}{20} \right) e^{-\left(\frac{x}{2} - \frac{t_w}{\tau_s}\right)} \right] \times \left(1 - e^{-\frac{x}{2}} \right). \quad (\text{A.5})$$

If the $t_1 \ll \tau_s$ and $t_1 \ll T_p$, Eq. (A.5) can be reduced to

$$\Phi(x) = \left(\frac{e^{-\frac{x}{20}}}{x} - \frac{e^{-\frac{x}{2}}}{x} + \frac{e^{-\frac{x}{2}}}{20} \right) \left(1 - e^{-\frac{x}{2}} \right). \quad (\text{A.6})$$

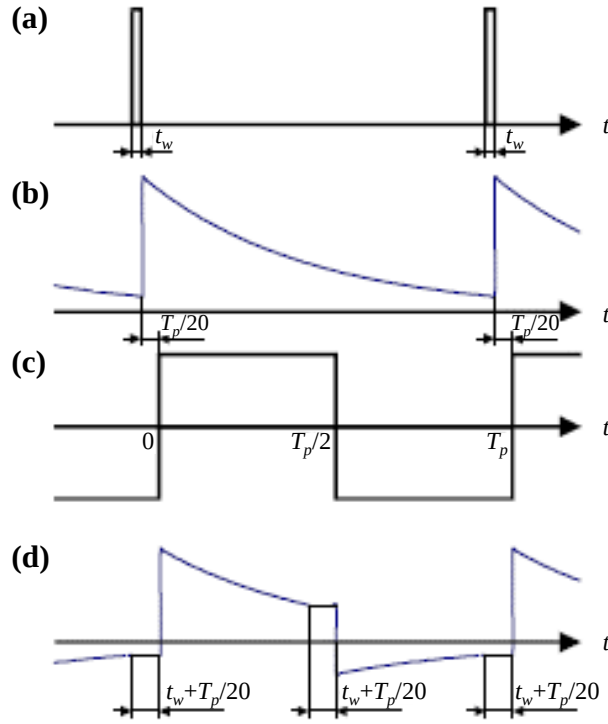


FIG. A.1 (a) Pulse voltage train, (b) capacitance transient, (c) lock-in function and (d) capacitance transient multiplied with the lock-in function [1].

Figure A.2 shows the lock-in function $\Phi(x)$, which is also called emission rate window.

$\Phi(x)$ has a peak when $x = 2.17$, whose value 0.18. The half-maximum of $\Phi(x)$ was 0.09 at $x = 0.5$ and $x = 7.5$.

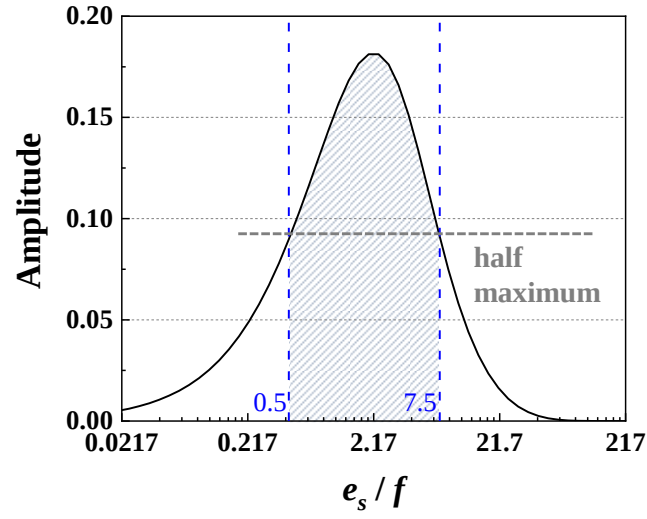


FIG. A.2 An emission rate window of the lock-in DLTS.

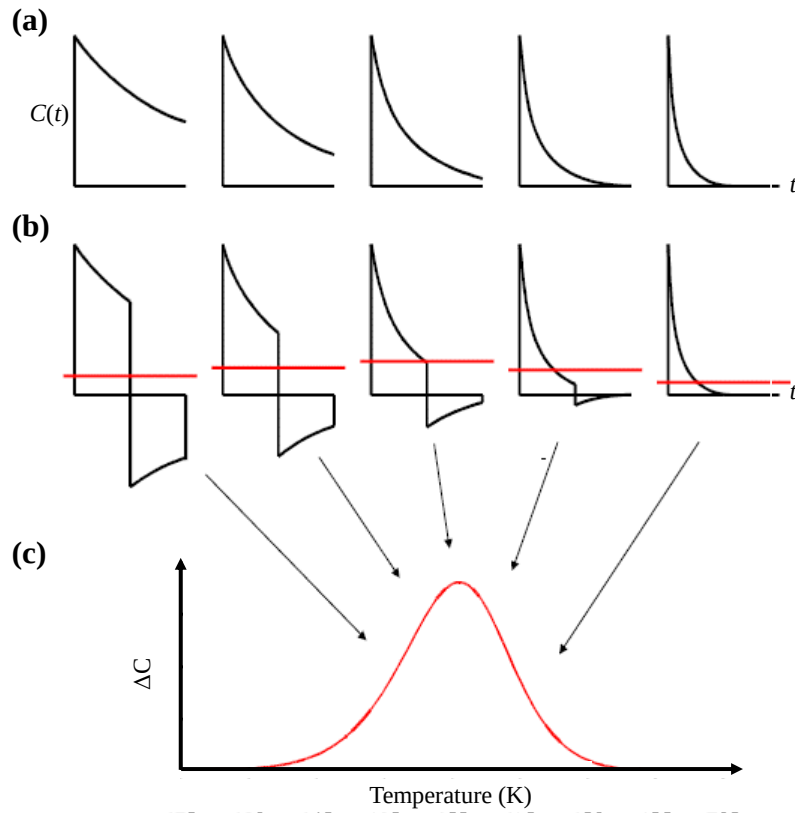


FIG. A.3 (a) capacitance transients with different emission time constants, (b) the capacitance

transients multiplied with the lock-in function, (c) DLTS spectrum of temperature scan [1].

To change the ratio of emission rate to frequency, temperature scan is commonly performed. A temperature scan DLTS spectrum is shown in Fig. A.3 [1]. The temperature is changed while the frequency is fixed during the measurement. The peak in the DLTS spectrum refers to the bulk traps contributing to energy level in the forbidden bandgap. Although the frequency scan, which is measured by changing the frequency while the temperature is fixed, also provides the traps information, temperature scan is more common, especially for IT analyses due to the wider range of energy distribution. In the case of ITs, the traps are distributed throughout the bandgap at the interface. Therefore, the spectrum we obtained is the peak sum, and ΔC at each temperature corresponds to the IT at a certain energy level.

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