

Reliability Assessment and Enhancement of Grid-Connected Renewable Energy onversion Systems

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Reliability Assessment and Enhancement
of Grid-Connected Renewable Energy
Conversion Systems

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Reliability Assessment and Enhancement of Grid-Connected Renewable Energy Conversion Systems

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Abstract

Recently, penetration levels of renewable energy sources in the electrical grids have been considerably increased and the need for high reliability and continuously available renewable sources has become important. However, field experience surveys conclude that the reliability of the interfacing power converters of renewable energy conversion systems represents a crucial factor for the existing and future extension of renewable sources in electrical power systems. Among different elements in power converters, power semiconductor devices possess the highest failure rates. Meanwhile, thermal stresses represent the most failure causing stressors in the elements of power converters.

Motivated by the abovementioned reliability problems of power semiconductor devices in renewable energy conversion systems (RECSs), the scope of this thesis is concerning to accurately assessment and considerably enhancement of the reliability of power electronic converters that are considered the most vulnerable parts in RECSs. The thesis consists of five chapters, which can be summarized as follows:

In chapter one, an introduction to reliability problems in renewable energy conversion systems, the most vulnerable parts, and the dominant stressors on power components are presented. In addition, problem definition, research motivations, and thesis outlines are introduced as well.

In chapter two, a more convenient approach for thermal behavior, and lifetime assessment for wind power converters is presented as a case study that considers the influence of the operating functionalities and operating environment of wind energy conversion systems (WECSs) in utility grids. The distribution static compensator (DSTATCOM) functionality, and various modes of resilient microgrids operation are considered in the selected case study. The feasibility of the proposed approach has been verified analytically and compared to the previously addressed approaches. By applying the proposed approach, more precise estimations of thermal stresses and lifetime consumption have been obtained with considering the stochastic behaviors of wind power and load demands in addition to operational characteristics of resilient microgrids.

In chapter three, a new method for enhancing the reliability of single phase power inverters through achieving relief of thermal stresses of stressed power semiconductor devices is proposed. The proposed method is a new carrier-based thermal stresses relief pulse width modulation (TSRPWM) strategy for extending the lifetime of semiconductor switches in single-phase multilevel inverters. It retains the same benefits as the conventional carrier pulse width modulation (PWM) methods, i.e., a simple and easy implementation, but presents a significantly reduced power

losses and thermal stresses of the stressed semiconductor devices. The proposed strategy benefits the inherent redundancy among switching states in multilevel inverters to optimally relieve the thermally stressed device. The proposed algorithm maintains the inverter operation without increased stresses on healthy switches and without reduction of the output power ratings. In addition, the proposed algorithm preserves voltage balance of the DC-link capacitors. The proposed strategy is validated on single phase five level T-type inverter system with considering different locations of thermal stresses detection. Experimental prototype of the selected case study is built to verify the results. Moreover, comparisons with the most featured strategies in literature are given in detail in the chapter.

In chapter four, another lifetime extension method for enhancing the reliability of three-phase power inverters is proposed. The proposed method is based on a novel space vector modulation (SVM) algorithm for lifetime prolongation of thermally-aged power semiconductor devices in multilevel inverters. The proposed SVM algorithm functions to alleviate the affected device and to prevent the harmful consequences such as short/open circuit faults. The proposed algorithm is generalized that can prolong any of power semiconductor device of n-level inverters independently from the number of output levels. The feasibility of the proposed method has been verified by simulation and experimental results on the three-phase three-level T-type inverter and compared to the previously addressed approaches. It can be concluded that the proposed algorithm provides a significant reduction of thermal stresses on the thermally-aged power devices in addition to maintaining the same components count, the same output ratings, the same output levels, and balanced capacitors' voltages as well.

Chapter five – the last chapter in the thesis – includes both the final summary and the conclusion outline for the thesis and the expected extended future work.

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Chapter 1

Introduction

1.1 Overview

With the increased penetration levels of renewable energy sources in the electrical grids, the need for high reliability and continuously available renewable energy sources has become important. In this chapter, the reliability and the main crucial elements to define it for grid connected renewable energy generation systems are analyzed. Additionally, the main stressors and failure causes are introduced. Power semiconductor devices, as the weakest element from the reliability point of view, are considered to assess and enhance the reliability of renewable energy conversion systems. The motivations and outlines of the thesis are introduced at the end of the chapter.

1.2 Introduction

Globally, the penetration levels of renewable energy sources into the electrical grid power systems are growing exponentially [1]. For instance, the annual growth rate of wind energy generation has been sharply increased reaching of 17.02% from 2014 to 2015, with expected increased worldwide capacity of 2000 GW by the year 2030 [2]. In addition, the yearly growth rate of photovoltaic (PV) generation has been largely increased reaching of total generation of 227 GW in 2015 compared with total generation of 177 GW in 2014. It is expected that PV generation continue increasing and achieving between 1760 to 2500 GW by the year 2030 [2]. In accordance, a vast improvement in renewable power

technologies has been achieved. An increased attention has been given to large-scale renewable energy systems that help to increase power densities and to decrease the cost of the generated kilowatt-hours [3]. Therefore, renewable energy conversion systems (RECSs) are required to play a more significant role in supporting electrical grids and self-healing capability of utility grids. The increased penetration level of RECSs has made their reliability, availability, and maximum energy harvesting of the principal interests for research and industry [4]–[6].

A schematic diagram of a typical structure and components in RECSs is shown in Fig. 1.1. Power electronics converters represent the main element in RECSs, wherein power electronics converters function to harvest the maximum energy of the source and handle the extracted energy from the renewable source into the electrical grid.

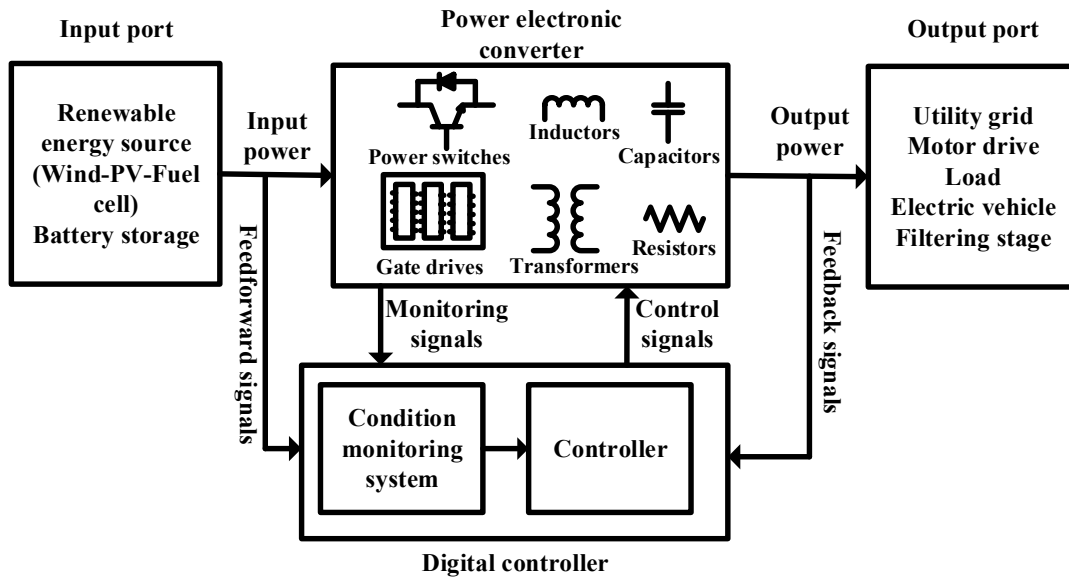


Fig. 1.1 Typical structure and components in renewable energy generation systems.

1.3 Reliability of Power Converters

1.3.1 Industry Based Reliability Surveys

Field experience based analysis of contribution of various components in RECSs, including PV systems and wind systems, shows that power electronic converters represent the most vulnerable parts [7]. Thence, power electronic converters are among the most critical elements in terms of high failure rates, shortened lifetime, and high maintenance costs.

Statistical analysis based on field experience of PV generation systems were provided in [8]–[10], wherein analysis shows that electrical converters represent the most reliability critical parts among various components in the PV generation system. Fig. 1.2 shows an overview of the contribution of various elements of PV generation systems in the unavailability of the whole PV system [8]. It is clear that PV inverters has the highest impact on PV system availability as they cause around 64% of the total failures in PV systems.

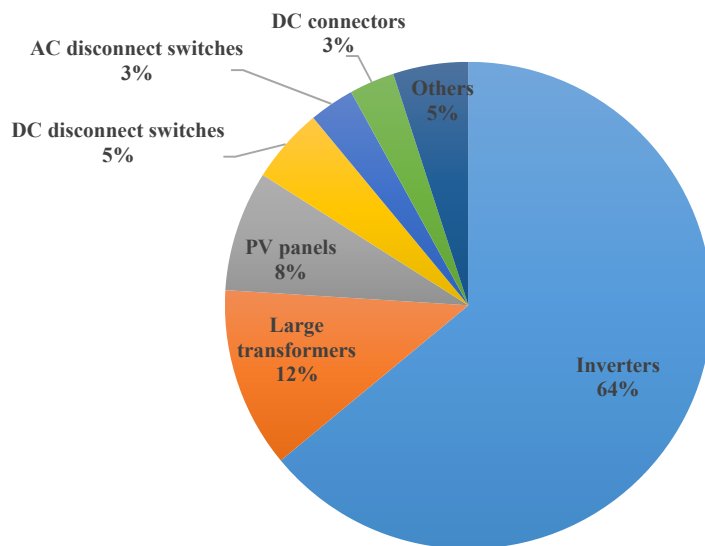


Fig. 1.2 Failure distribution among various components in PV generation system [8].

Fig. 1.3 shows the annual failure rate and downtime per failure of the different components in wind generation systems [11]. The analysis is based on field data of more than 6000 onshore wind generation system for around 11 years. It is clear that the electrical system possesses the highest failure rate in the wind generation system. Another field experience study has been introduced in [12], wherein power electronic converter failure frequency is about 13 % of the overall normalized failure rate and also power converters cause 18.3 % of the normalized overall downtime of the studied wind turbines.

It can be concluded from the aforementioned industry-based reliability surveys that power electronics converters are among the major parts in terms of expected lifetime and reliability of wind and PV generation systems.

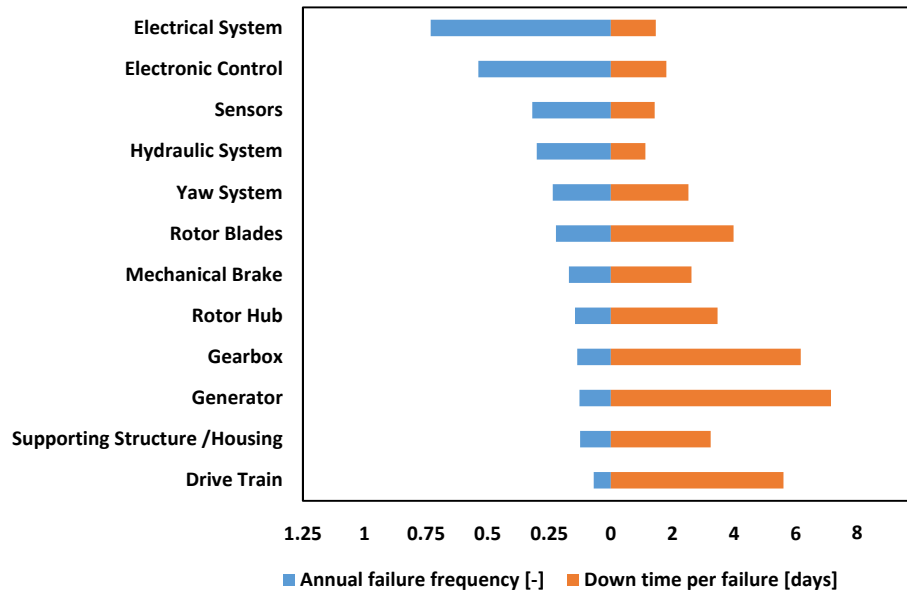


Fig. 1.3 Annual failure frequency with downtime for various components in wind generation system [11].

In addition, the contribution of the different components in failures of power converters has been widely analyzed in the literature, wherein the power semiconductor devices

possess the highest failure rates. Fig. 1.4 shows the percentage contribution of different components in total energy conversion system failure rates [13]. Semiconductor components are responsible for 21% of the total system failures. Therefore, reliability should receive higher attention when designing and developing renewable energy systems to avoid grid disturbances and power fluctuations.

Additionally, Fig. 1.5 shows the distribution of different failure stressors of power electronics systems [14]. It is evident that thermal stresses represent the dominant factor that lead to most of the power electronic system failures. Thermal stressors include the steady state and cycling temperatures of the device, which result from continuous loading and mission profiles of the operating environment. Stimulated by the abovementioned statistical and field operating surveys of RECSs, the assessment and enhancement of reliability of power electronic system is crucial and further investigations are required in this area and they will be covered in the thesis.

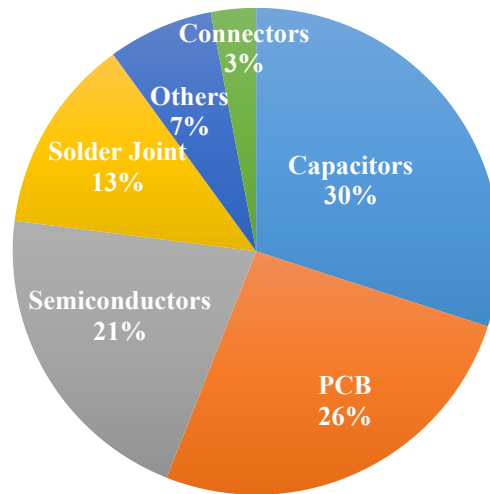


Fig. 1.4 Failure rates of different components of RECSs [13].

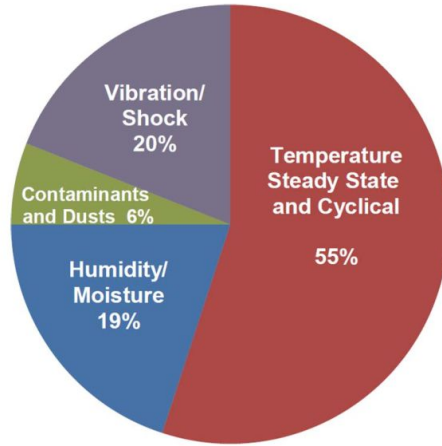


Fig. 1.5 Distribution of stressors that cause failures in power electronic system [14].

1.3.2 Insulated Gate Bipolar Transistor (IGBT) Construction

Power semiconductor devices represent the main cause of RECSs failures and hence they are considered the most important element to define the reliability of the RECSs. Power insulated gate bipolar transistors (IGBTs) devices are widely used in medium and high power applications. Fig. 1.6 shows the internal layers that structure IGBT devices [15]. Power IGBT devices are subjected to varying junction temperature due to continuous varying mission profiles of RECSs (solar irradiance and ambient temperatures in PV systems or wind speed and ambient temperature in WECSs). Whereas power IGBTs contain several materials with different mismatched coefficients of thermal expansion (CTE) that causes degradation in bond wire and in die attach [16]. Moreover, power IGBTs may fail without degradation due to large surges and transients. Therefore, developing an effective methods for prolonging the lifetime of power semiconductor devices can improve the reliability and availability of the whole RECSs through relieving and thermal control

of degraded devices. The scheduled maintenance and replacement programs can be set accurately as a consequence.

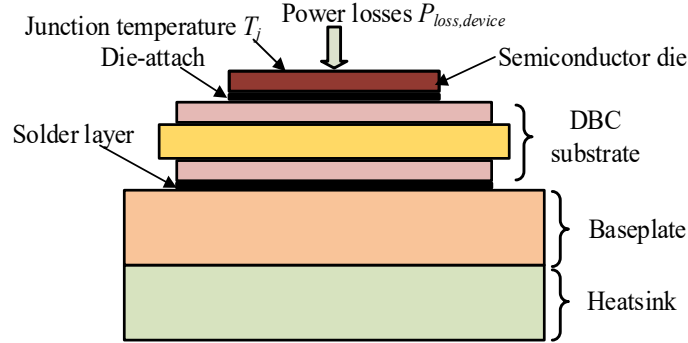


Fig. 1.6 Thermal stresses and structure of different layers in IGBT devices [15].

1.3.3 Reliability Related Models of Power IGBTs

The operating mission profiles of power converters are transferred into different loading on their power semiconductor devices. Normally, power losses through power devices are dissipated into the air through heatsinks. Then, the operating lifetime of the power converter is defined according to the amount and the duration of the loading. Fig. 1. 7 shows the relation between various models of power IGBT devices. The gating signal and power loading generate power losses through the device. Then, thermal models of the device are used to transfer the power losses through the device into thermal stresses. The thermal behavior is depicted by junction temperature T_j and junction temperature fluctuation ΔT_j of power semiconductor devices. Finally, thermal stresses with the help of lifetime models of power devices such as Coffin-Manson rule [17] and Miner rule [18] provide the remaining useful lifetime (RUL) of the power converters.

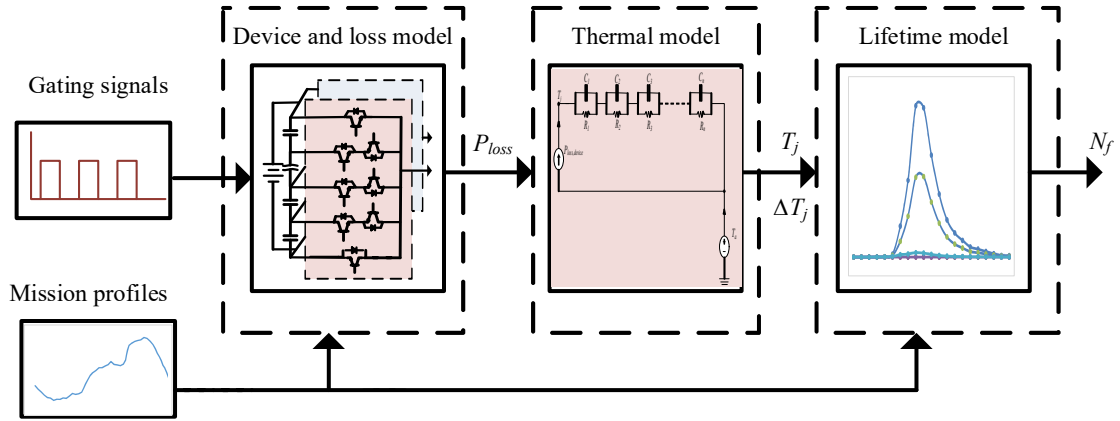


Fig. 1.7 Relationship between various models of power IGBT devices.

1.4 Problem Definition

It is clear from the aforementioned discussion that the reliability of the interfacing power converters of renewable energy conversion systems represent a crucial factor for the existing and future extension of renewable sources in electrical power systems. According to field experience surveys, power semiconductor devices possess the highest failure rates among the different elements in power converters. Meanwhile, thermal stresses represent the most failure causing stressor in the elements of power converters. However, high reliability and availability of renewable energy systems are highly needed to avoid unscheduled shutdown periods and to decrease maintenance and repairing costs of renewable energy conversion systems. For that reason, accurate assessment of reliability of power converters in renewable energy application with considering the various operating modes and configuration is needed. Moreover, investigating lifetime extension methods through controlling the thermal stresses of power semiconductors in power converters with maintaining the full output ratings represents a major element in increasing the availability

of renewable energy conversion systems. The investigated methods for reliability assessment and enhancement are introduced in the next section.

1.5 Research Objectives

Motivated by the abovementioned reliability problems of power semiconductor devices in renewable energy conversion systems, the scope of this thesis is concerning to accurately assessment and considerably enhancement of the reliability of power electronic converters that are considered the most vulnerable parts in RECSs.

In order to overcome the limitations of the existing reliability estimation techniques, a new method is developed for assessing the reliability of power converters in wind energy conversion systems, as a case study. The proposed method considers the stochastic behaviors of both wind power and load demands in electrical power systems. Moreover, the proposed method provides an accurate evaluation of the associated thermal stresses and reliability issues of power converters in WECS with considering the required functionalities of power converters to achieve resilient operation of modern utility grids. Moreover, the proposed approach provides a generalized methodology that considers different topological, configurational, and functionalities changes of WECS and various requirements of power systems with WECS integration, which is considered one of the main salient characteristics featured by the proposed approach.

Moreover, two new methods are developed to extend the lifetime of power converters in single and three-phase grid connected renewable energy systems through managing and reducing the thermal stresses of power semiconductor devices. The proposed methods rely on developing new pulse width modulation (PWM) methods to alleviate thermally stressed semiconductor devices in single- and three-phase power inverters. The proposed

algorithms provide the benefits of: simple implementation without increased complexity at higher number of levels of power inverters; no need for output ratings compromise; cheap solution without extra system cost. In addition, the proposed strategies ensure high performance regarding voltage balance of DC-link capacitors of multilevel inverter.

1.6 Research Outlines

The Thesis is divided into five chapters. The outlines of these chapters are as follows:

In chapter one, an introduction to reliability problems in renewable energy conversion systems, the most vulnerable parts, and the dominant stressors on power components are presented. In addition, problem definition, research motivations, and thesis outlines are introduced as well.

In chapter two, a more convenient approach for thermal behavior, and lifetime assessment for wind power converters is presented, as a case study, that considers the influence of the operating functionalities and operating environment of wind energy conversion systems (WECSs) in utility grids. The distribution static compensator (DSTATCOM) functionality, and various modes of resilient microgrids operation are considered. The feasibility of the proposed approach has been verified analytically and compared to the previously addressed approaches. By applying the proposed approach, more precise estimations of thermal stresses and lifetime consumption have been obtained with considering the stochastic behaviors of wind power and load demands in addition to operational characteristics of resilient microgrids.

In chapter three, a new method is proposed for enhancing the reliability of single phase power inverters through achieving relief of thermal stresses of stressed power

semiconductor devices. The proposed method is a new thermal stresses relief carrier-based pulse width modulation (TSRPWM) strategy for extending the lifetime of semiconductor switches in single-phase multilevel inverters. It retains the same benefits as the conventional carrier pulse width modulation (PWM) methods, i.e., a simple and easy implementation, but presents a significantly reduced power losses and thermal stresses of the stressed semiconductor devices. The proposed strategy benefits the inherent redundancy among switching states in multilevel inverters to optimally relieve the thermally stressed device. The proposed algorithm maintains the inverter operation without increased stresses on healthy switches and without reduction of the output power ratings. In addition, the proposed algorithm preserves voltage balance of the DC-link capacitors. The proposed strategy is validated on single phase five level T-type inverter system with considering different locations of thermal stresses detection. Experimental prototype of the selected case study is built to verify the results. Moreover, comparisons with the most featured strategies in literature are given in detail in this chapter.

In chapter four, another lifetime extension method for enhancing the reliability of three-phase power inverters is proposed. The proposed method is based on a novel space vector modulation (SVM) algorithm for lifetime prolongation of thermally-aged power semiconductor devices in multilevel inverters. The proposed SVM algorithm functions to alleviate the affected device and to prevent the harmful consequences such as short/open circuit faults. The proposed algorithm is generalized that can prolong any of power semiconductor device of n -level inverters independently from the number of output levels. The feasibility of the proposed method has been verified by simulation and experimental results on the three-phase three-level T-type inverter and compared to the previously

addressed approaches. It can be concluded that the proposed algorithm provides a significant reduction of thermal stresses on the thermally-aged power devices in addition to maintaining the same components count, the same output ratings, the same output levels, and balanced capacitors' voltages as well.

Chapter five – the last chapter in the thesis – includes both the final summary and the conclusion outline for the thesis and the expected extended future work.

Chapter 2

Thermal and Reliability Assessment for Wind Energy Systems with DSTATCOM Functionality in Resilient Microgrids

2.1 Overview

Different functionalities can be incorporated into wind energy conversion systems (WECSs) in resilient microgrids in order to reduce the total system cost and to assist their self-healing capability. Meanwhile, wind industry-based reliability surveys have addressed that power electronics components are the most vulnerable parts in WECS. Therefore, thermal stresses and lifetime consumption of WECS are critical factors for evaluating the added functionalities and for developing new control strategies as well. Almost all of the previous methodologies in the literature tackle the problem of lifetime assessment of WECS using only the behavior of wind generation profiles and reactive power injection, which is limited by grid codes. Subsequently, these approaches cannot efficiently achieve lifetime assessment in case of resilient microgrid operation and different load demands. This chapter proposes a more convenient approach for thermal behavior, and lifetime assessment for WECSs that considers the influence of the added DSTATCOM functionality, and various modes of resilient microgrids operation. The feasibility of the proposed approach has been verified analytically and compared to the previously addressed approaches.

2.2 Introduction

2.2.1 Neutral Point Clamped Inverters and Resilient Microgrids

Recently, an increased attention has been given to large-scale wind energy systems that help to increase power densities and to decrease the cost of the generated kilowatt-hours [3]. Therefore, wind energy conversion systems (WECSs) are required to play a more significant role in supporting electrical grids and self-healing capability of resilient microgrids. More strict requirements have been arising for WECS in microgrids operations that put their failures or unavailability undesirable [19]. Therefore, reliability and lifetime consumption with the added functionalities and requirements have been greatly highlighted.

Recently, neutral-point-clamped (NPC) inverters topologies have become promising solutions in high power applications compared to conventional two-level inverters [20]. However, they are considered the most crucial elements in terms of contribution to total system failures and unavailability. Therefore, achieving a more reliable operation is highlighted from the perspective of wind power industry. Thermal stresses are the major stressors of system failure and unavailability with 55% portion among stressors distribution of power components [7]. This can be interpreted as power semiconductor devices are composed of layers of different materials and therefore they have different thermal expansion coefficients. Hence, continuous overloading and power cycling result in cracks, voids, and delamination of power devices components [21].

To comply with the grid-side commands, full-scale WECSs equipped with permanent magnet synchronous generators (PMSG) have become more prevalent in megawatt (MW) wind energy scale in terms of increased efficiency, and enhanced grid supportability [14].

However, they require full-scale power conditioning that result in high power losses and increased system complexity [22]. Significant impacts on utility grids appeared with the increased wind parks and wind penetration levels. Since WECS are tied to the electrical grid in transmission and distribution levels, they are appealed to practice like conventional generation and to assist in supporting the reactive power into the utility grid. Though, this reactive power support leads to additional power losses and hereby thermal stresses in power components of wind power inverters [23]. Fig. 2.1 shows the different operating modes of power inverters in resilient microgrids. Two grid-connected separate inverters are used in Fig. 2.1(a) to perform as wind active power injection (grid-connected wind inverter) and to perform DSTATCOM functionality (grid-connected DSTATCOM inverter) into the electrical grid. A single inverter is utilized in Fig. 2.1(b), and (c) for wind active power injection with DSTATCOM functionality in grid-connected mode (grid-connected and combined wind+DSTATCOM inverter), and in islanded mode (islanded and combined wind+DSTATCOM inverter), respectively.

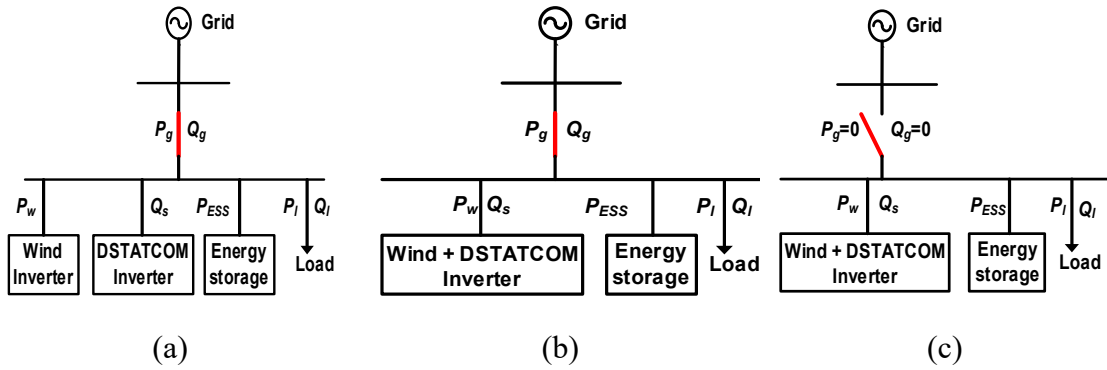


Fig. 2.1. Different operating modes of power inverters in resilient microgrid a) Grid-connected and separate (wind inverter and DSTATCOM inverter) b) Grid-connected and combined wind+DSTATCOM inverter, and c) Islanded and combined wind+DSTATCOM inverter.

The utilization of multi-functionality WECS in resilient microgrids helps to decrease the initial system cost and to increase the supportability provided by WECS in the resilient mode of operation. However, increased complexity of the controller and extra stresses on the power electronics components are expected. In resilient microgrids operation of WECS, the situation is more severe due to the stochastic behavior of wind generation, and load demands. In addition, resilient microgrids are subjected to operate in grid-connected and resilient modes of operation. Therefore, a more precise assessment of thermal behavior and lifetime consumption is highly required to evaluate economic impacts of the added functionalities and to develop more efficient controllers as well.

2.2.2 Existing Issues of Reliability Assessment Methods

Several studies have been presented in the literature for reliability assessment of power electronics components [24]–[32]. Conventional reliability models such as ML-HDBK [24], and PRISM [25] rely on assembled field data of failures and assumed constant failure rate for power semiconductor devices. However, different loading and environmental operating conditions are ignored in this type of reliability analysis. In addition, this model presents a restricted interpretation for faults and reliability issues. Reliability tests performed by power device manufacturers also give considerable information about component consumption and causes. Although, the lack of generality and negligence of field operating data are the main disadvantages of these types of reliability tests. Another more realistic lifetime consumption models have been developed using collected field data of wind speeds and ambient temperature [26]–[32].

In [26], the authors summarized the main factors affecting the reliability of power semiconductor devices. These factors are the junction temperature, temperature cycling,

and the duration time of ON-state of output current. In [27], the thermal loading on wind power converters have been classified into long-term, medium-term, and short-term profiles resulting from operational wind power and ambient temperature. A method for predicting bond wire fatigue failures of power semiconductor devices in photovoltaic (PV) inverters using their long-term irradiance profiles has been presented in [28]. Reliability comparisons between GaN HEMTs and Si IGBTs for long-term operation of PV inverters have been introduced in [29]. However, these methods only consider the stochastic behavior of generation-side and ignore the dependency of lifetime consumption on load-side demands and different modes of operation.

On the other hand, the situation is totally different in doubly fed induction generators (DFIG)-based WECS as both of the rotor-side converter and grid-side converter are able to support the reactive power injection. An optimized power losses methodology to balance the lifetime of the two converters of DFIG-based WECS through optimum share between the two converters has been presented in [30]. Another reactive power dispatch method for lifetime improvement of DFIG-based wind farms under wake effect has been presented in [31]. In [32], different thermal stresses due to injection of reactive power in night periods for single-phase photovoltaic (PV) inverters have been analyzed.

The control of PV inverter as STATCOM device has been introduced in [33], and a modular multilevel inverter topology for wind generation that capable of providing the function of flexible AC transmission system (FACTS) has been introduced in [19]. The design of the inverter and controller parameters for PV-STATCOM have been presented in [34]. A method for injecting local reactive power demand to reduce feeder losses by means of electronic tap changer of the transformer has been introduced in [35]. Moreover,

another method for improving full-range control of reactive power injection of PV-inverters has been presented in [36]. An analytical approach for achieving maximum grid support of grid-connected inverters with injecting the maximum allowable active and reactive power has been provided in [37]. However, the associated thermal behavior and lifetime consumption of power semiconductor devices for this operation of inverters have not been investigated in the literature.

2.2.3 Contribution

This chapter addresses the thermal behavior and reliability assessing for three-level NPC wind power inverters used in resilient microgrids with DSTATCOM functionality. Particularly, thermal stresses and reliability at different operating modes of resilient microgrids are analyzed. In addition, the stochastic behavior of different wind power and load demands are considered. Table 2.1 compares the main features of the proposed approach with the previously addressed approaches. The superiority and novelty of the proposed approach are summarized as follows:

- The proposed approach provides a novel methodology for lifetime consumption assessment for multilevel inverters in WECS with DSTATCOM functionality that combines the stochastic behaviors of both wind power and load demands. This is the first time such joint stochastic behaviors are considered.
- The proposed approach provides a new assessment approach of the thermal stresses and reliability issues of power converters in WECS with the added DSTATCOM functionality considering different operating modes of resilient microgrids.
- The proposed approach provides a generalized methodology that considers different topological, configurational, and functionalities changes of WECS and various

requirements of systems with WECS integration, which is considered one of the main salient characteristics featured by the proposed approach.

This chapter is organized as follows: Section 2.3 introduces the details of the focused case study and the inverter loading profiles modeling at different operating modes. Afterward, Section 2.4 presents the probabilistic-based lifetime assessment methodology for power semiconductor devices of NPC inverters in resilient microgrids. Section 2.5 addresses the analytical calculations for power losses and thermal profiles at different operating modes. Furthermore, the obtained results are shown and compared. Section 2.6 presents the assessment and comparison of NPC inverters' lifetime at different operating modes. Section 2.7 summarizes the practical considerations for generalizing the proposed approach. Finally, Section 2.8 remarks concluding commentary.

Table 2-1

Comparison of the proposed approach with existing studies in the literature

Reference	Contribution	Configurational changes	Reactive power injection handling	Stochastic behavior consideration	Multi-functionality handling	Resilient microgrids considerations
[24], [25]	Reliability assessment using assembled field data of failures	√	×	×	×	×
[26]	Study the main factors affecting reliability	√	×	×	×	×
[27]–[29]	Lifetime assessment at different wind profiles	√	×	×	×	×
[30], [31]	Reliability assessment for DFIG at different Q share between converters	×	√	×	×	×
[32]	Effect of Q injection outside feed-in times of PV systems	√	√	×	×	×
Proposed	Reliability assessment considering stochastic behavior of wind power and load demand in resilient microgrids	√	√	√	√	√

2.3 Selected Case Study and Inverter Loading Profiles

2.3.1. Structure of the Selected Case Study

Fig. 2.2. shows the configuration of a 2 MW geared PMSG-based WECS with back to back (B2B) three-level NPC inverter. In B2B configuration, controlling generator-side rectifier and grid-side inverter can be performed separately. The used controller is implemented using the synchronous d-q reference frame provided in [38]. Controlling active and reactive powers is done by setting the d-axis and the q-axis reference currents, respectively. In addition, the grid-side inverter in resilient microgrids operation is subjected to operating in grid-connected mode or islanded mode. Therefore, different thermal stresses are expected on power semiconductor devices of the grid-side inverter, whereas thermal stresses in generator-side rectifier remain the same. The basic parameters for the selected grid-side inverter for case study are summarized in Table 2.2.

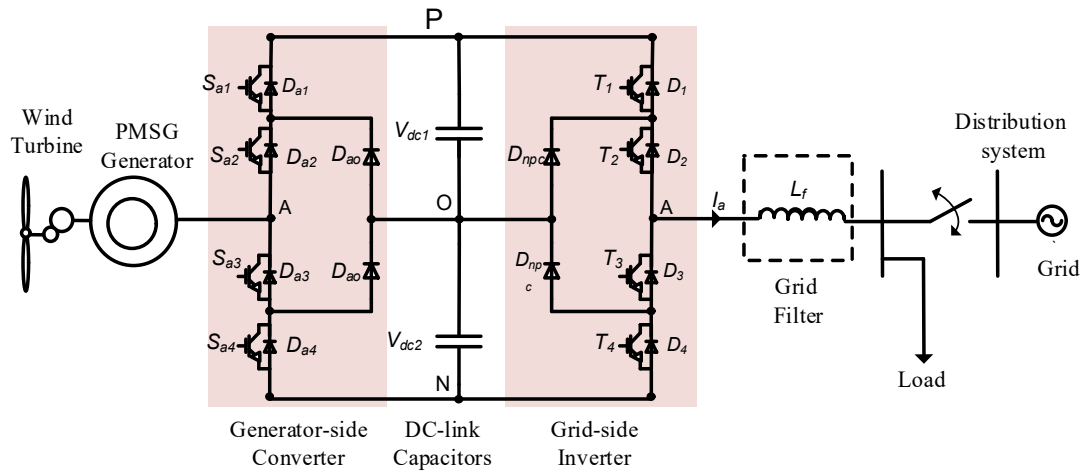


Fig. 2.2. Single-phase representation of B2B NPC inverter wind generation for distribution microgrid.

2.3.2. Wind Turbine

The selected case study depends on using 2050 kW Enercon wind turbine in resilient microgrid system. The wind generator generates electrical power during wind speed regions between cut-in V_{ci} and cut-off V_{co} speeds. The rated wind speed for the selected case study equals to 12 m/s with wind class I distribution. The output power curve of 2050 kW wind turbine at different speeds used throughout this chapter is shown in Fig. 2.3 [39].

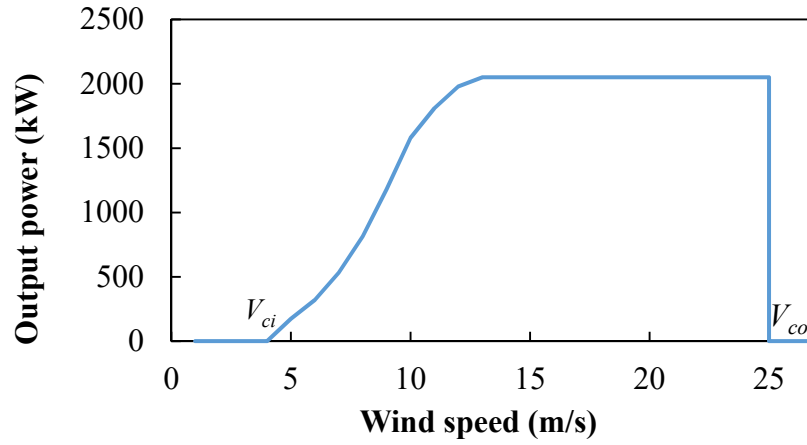


Fig. 2.3. The output power P_{wind} of Enercon 2050 kW wind turbine at different wind speeds [39].

2.3.3. Loading Profiles of Wind Inverter

The NPC inverter is subjected to different loading profiles in resilient microgrid operation due to the previously described four modes of operation (grid-connected wind inverter, grid-connected DSTATCOM inverter, grid-connected and combined wind+DSTATCOM inverter, and islanded and combined wind+DSTATCOM inverter). Loading profiles of NPC inverter depend on their functions to transfer the generated active power and/or reactive power into the microgrid load at different operating modes. Adding DSTATCOM

functionality eliminates the need for capacitor banks or separate DSTATCOM devices to supply the needed reactive power.

The grid-connected wind inverter with combined wind+DSTATCOM functionalities has to provide control for the injected active power P_w of the wind and reactive power Q_s into the grid independently. In case there is no-generated active power (wind speed V_i less than cut-in speed V_{ci} and wind speed more than cut-off speed V_{co}), the inverter has to operate as a capacitor bank and hence performs the function of DSTATCOM. This operation imposes different loading effects on semiconductor devices that have to be properly defined to evaluate their corresponding power losses. In grid-connected operation, the limit of the injected reactive power into the grid is restricted by predefined range given by grid codes $Q_{grid,limit}$ (which equals to 0.23 p.u. in the selected case study according to grid codes in [40]). Whereas, the reactive power injection is limited by load demands of reactive power Q_{load} in the islanded operation.

The loading profiles of combined wind+DSTATCOM inverter in grid-connected mode are expressed as follows:

$$\text{Loading Profile} = \begin{cases} P_w = 0 & \text{and } Q_s \leq Q_{grid,limit} \\ & \text{if } V_i \leq V_{ci} \text{ or } V_i \geq V_{co} \text{ DSTATCOM – Mode} \\ P_w = P_{wind} & \text{and } Q_s \leq Q_{grid,limit} \\ & \text{if } V_{ci} < V_i < V_{co} \text{ Inverter Mode} \end{cases} \quad (2.1)$$

whereas, loading profiles in islanded mode are:

$$\text{Loading Profile} = \begin{cases} P_w = 0 & \text{and } Q_s = Q_{load} \\ & \text{if } V_i \leq V_{ci} \text{ or } V_i \geq V_{co} \text{ DSTATCOM – Mode} \\ P_w = P_{wind} & \text{and } Q_s = Q_{Load} \\ & \text{if } V_{ci} < V_i < V_{co} \text{ Inverter Mode} \end{cases} \quad (2.2)$$

From (2.1), and (2.2), it can be concluded that the maximum loading of reactive power is defined according to the operating mode whether it is grid-connected or islanded mode. The relationship between the injected active power P_w and reactive power Q_s with the inverter output voltage E_{inv} and the utility grid voltage E_g is as follows:

$$P_w = -\frac{E_{inv} * E_g}{X_f} \sin \delta \quad (2.3)$$

$$Q_s = -\frac{E_{inv} * E_g * \cos \delta - E_g^2}{X_f} \quad (2.4)$$

where X_f is the inductive reactance between the inverter and grid and it is considered equal to filter reactance for simplicity of calculation. Whereas, δ represents the displacement angle between E_{inv} and E_g . From (2.3) and (2.4), the active and reactive power flow between the inverter and the utility grid are performed by controlling the inverter output voltage E_{inv} and the displacement angle δ . The output voltage of the inverter is adjusted through the modulation index of the inverter.

2.3. 4. Modeling of Joint Wind Power-Load Demand Distribution

Due to the stochastic behavior of wind power distribution, the recorded historical data at the installation site can be used to determine the probability of wind speed to be in particular level within defined increment. The statistical behavior of wind distribution can be described in terms of their probability distribution function (PDF). These PDFs are composed of the different probability of a certain wind speed $Prob(V_i)$, which is a representation of the annual percentage contribution of wind speed V_i in the total wind profile (% contribution in 8760 hours). Wind profiles are categorized into Class I, Class II, and class III by the IEC standard. The three categories have mean wind speeds of 10, 8.5, and 7.5 m/s, respectively. Based on the recommended operating average speed of the

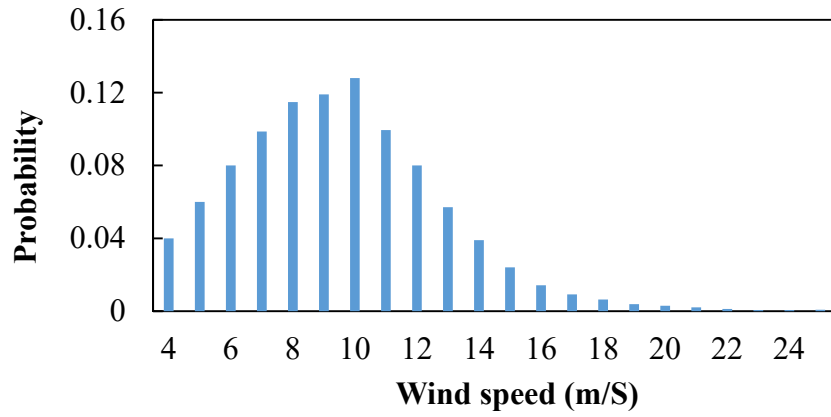
selected wind turbine, a Weibull-based class I wind distribution is well-suited. PDF of the annual wind speed for the selected case study is expressed using the Class-I wind distribution with wind speed increment of 1 m/s as shown in Fig. 2.4(a) [30].

The stochastic behavior of the load demand has to be considered for better prediction of the lifetime of the semiconductor devices. Similarly, the PDF of the load demand can be extracted from the recorded databases in the utility company. Studies for accurate planning of power systems have recommended using hourly load profiles of the IEEE-RTS [41]. In accordance, the load demand L_j is clustered into ten levels with corresponding ten probabilities $Prob(L_j)$ for the selected case study as shown in Fig. 2.4(b) [42]. The load demand power factor (PF) is assumed to be constant for the simplicity of calculations in the case study.

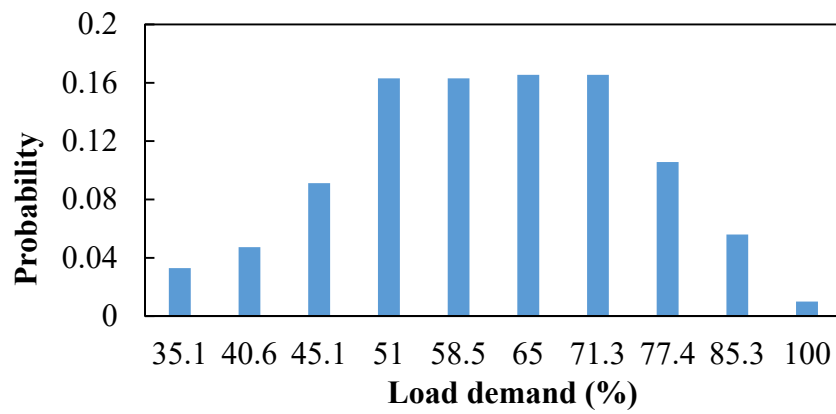
The previously pointed out probability models for wind power and load demand are employed to develop a joint probabilistic wind power and load demand models. It is assumed that there is no correlation between the two probabilities in this analysis. The joint probability $Prob(V_i, L_j)$ between any combination of wind power and load demand is:

$$Prob(S_n) = Prob(V_i, L_j) = Prob(V_i) * Prob(L_j) \quad (2.5)$$

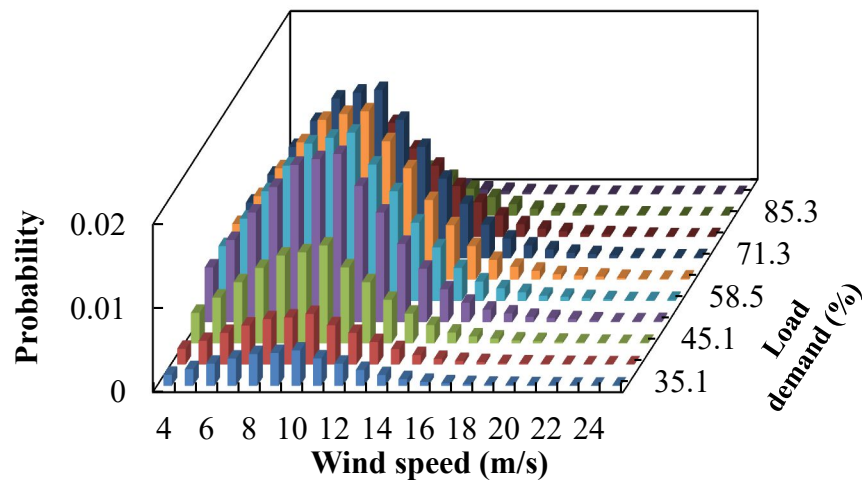
Therefore, a complete joint wind power and load demand model can be acquired by listing all the probable set S_n of the load demand probability and the wind power generation probability. Fig. 2.4(c) shows the joint probability distribution function (JPDF) of combined probabilistic wind power-load demand model that is used during the selected case study.



(a)



(b)



(c)

Fig. 2.4. The probabilistic model for the selected case study a) Wind power PDF, (b) Load demand PDF, and (c) Combined wind power and load demand JPDP.

2.4 Lifetime Assessment Methodology for NPC Inverter

2.4.1 Overview of the Proposed Approach

Fig. 2.5 shows the main steps for lifetime assessment for power semiconductor devices in NPC wind inverters with DSTATCOM functionality. The estimation process contains three main steps. Firstly, combining different probabilities of (wind power, and loads) of resilient microgrid operation, which are transferred into active and reactive power demands. This step can be done by collecting the loading profiles of NPC inverter based on wind power distribution and load demand distribution using gathered field data and establishing wind-load JPDF. The active power for each state is obtained from the relationship of wind turbine output power and wind speed. Whereas, the reactive power can be obtained based on the load percentage. Secondly, active and reactive power demands are transferred into thermal stresses with the help of loss model and thermal model of power semiconductor devices. The thermal behavior is depicted by junction temperature T_j and junction temperature fluctuation ΔT_j of power semiconductor devices for all the probable elements in set S_n of the system. Thirdly, lifetime consumption assessments are done by using Coffin-Manson rule [17] and Miner rule [18], which rely on JPDF of the loading profile. This can be transformed into useful information for control and design engineers and comparisons of the system lifetime with conventional solutions as well.

2.4.2 Generalized Implementation of the Proposed Approach

Based on the aforementioned overview of the proposed approach, a generalized implementation framework can be settled that is valid for various renewable energy systems and for different added functionalities as follows:

- 1- Obtain PDF of the renewable energy sources considering their properties and uncertainties of the available data.
- 2- Obtain PDF of the load demand side considering the characteristics of different loads and uncertainties of the available data.
- 3- Construct JPDF of the renewable source profile and load demand profile counting for their correlation if exist.
- 4- Calculate the loading profiles of different system components based on ratings and configuration of the system in addition to the desired functionalities of the system.
- 5- Based on the calculated loading profiles, select power semiconductors and various system components among those available in the market.
- 6- Construct power losses, thermal, and lifetime models of the selected devices using their manufacturers' datasheets or using standard tests in the literature.
- 7- Calculate power losses and thermal stresses of power devices for the operating loading profiles of the system.
- 8- Calculate lifetime consumption for various devices using their thermal stresses and operating JPDF.
- 9- Compare different operating modes and conditions in order to select the optimum operation of the system and to assess the feasibility of various added functionalities to the renewable energy system.

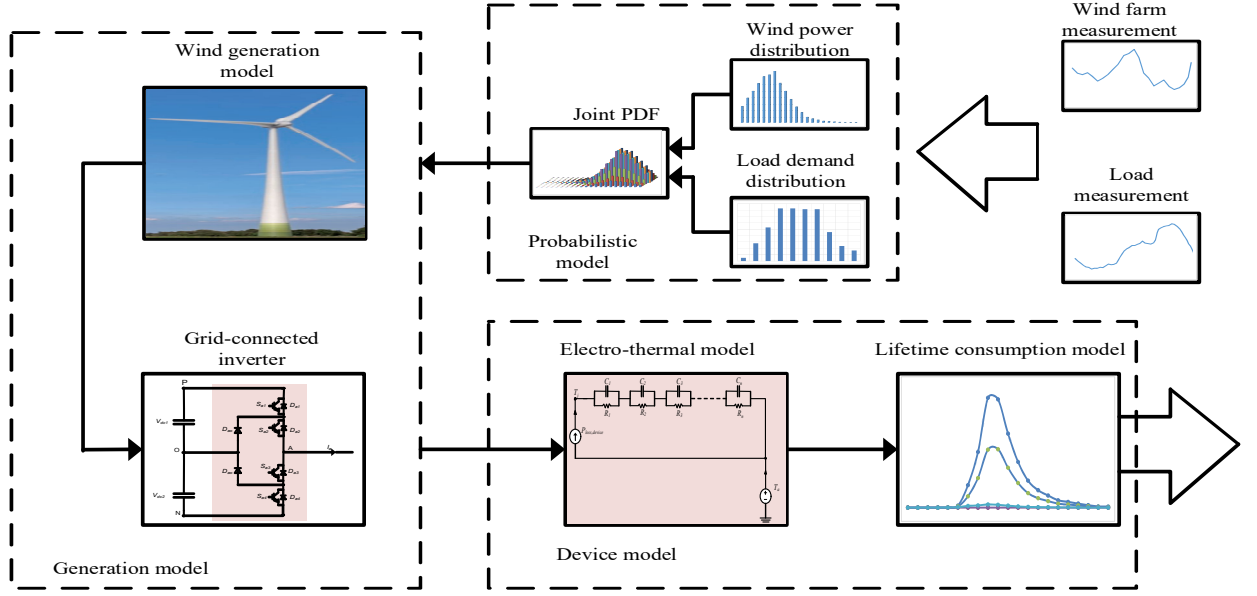


Fig. 2.5. Flowchart of the proposed probabilistic-based lifetime assessment methodology.

2.5 Thermal Behavior Analysis

2.5.1 Loss Calculation

Power losses in semiconductor devices are mainly resulting from two causes: (1) conduction losses, and (2) switching losses. The total power losses in a single semiconductor device $P_{loss,device}$ during switching period T_s ($=1/f_s$) are formulated as:

$$P_{loss,device} = P_{con,device} + P_{sw,device} \quad (2.6)$$

where $P_{con,device}$ is the power loss due to conduction, and $P_{sw,device}$ is the power loss resulting from switching the device ON and OFF. The analytical estimations of power losses in power semiconductor devices are given in details in [43]. The calculation method relies on using the detailed parameters that are available in devices datasheets given by manufacturers.

Based on the parameters of the selected case study in Table 2.2 and the parameters of power semiconductor devices, the simulations, and calculations of the system are performed using MATLAB environment. Fig. 2.6 shows and compares the power losses for power semiconductor devices of NPC inverter at extreme operating conditions for different operating modes. The comparison includes the four operating modes of NPC inverters in resilient microgrids; grid-connected wind inverter, grid-connected DSTATCOM inverter, grid-connected and combined wind+DSTATCOM inverter, and islanded and combined wind+DSTATCOM inverter. The wind inverter with DSTATCOM functionality supporting reactive power in islanded mode dissipates more power losses in semiconductor devices T_1 , T_2 , and D_{npc} . Whereas, the grid-connected DSTATCOM inverter operation without active power injection represents the lowest power losses in power semiconductor devices of NPC inverter among different extreme operating conditions. The variations of power losses in accordance to different wind speeds for different operating modes of NPC inverter in resilient microgrid operation are shown in Fig. 2.7 for the most stressed components T_1 , T_2 , and D_{npc} .

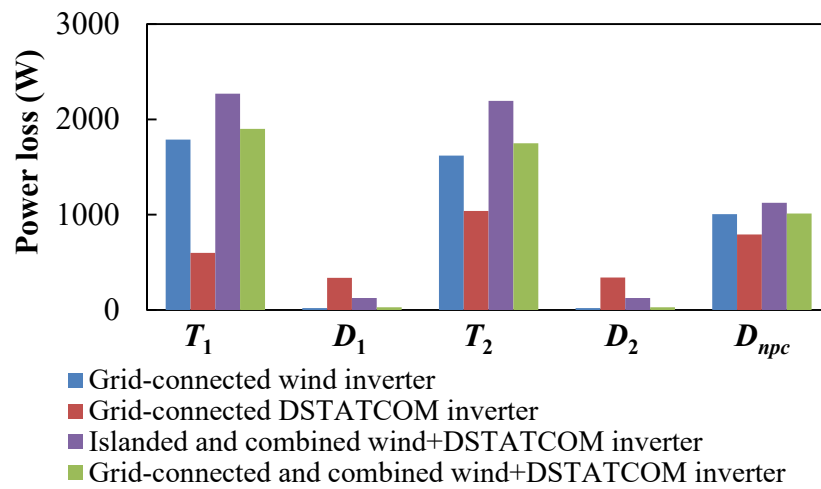
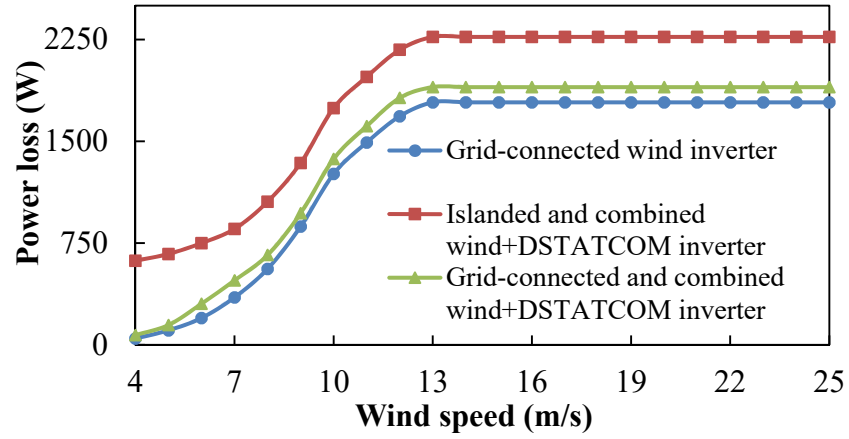
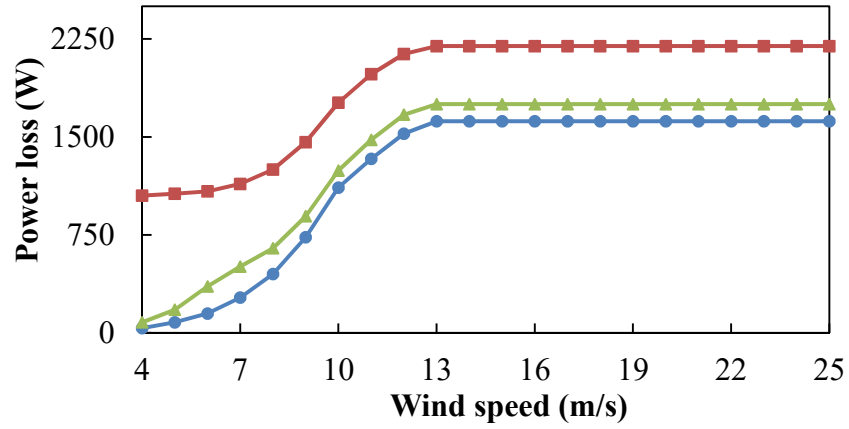


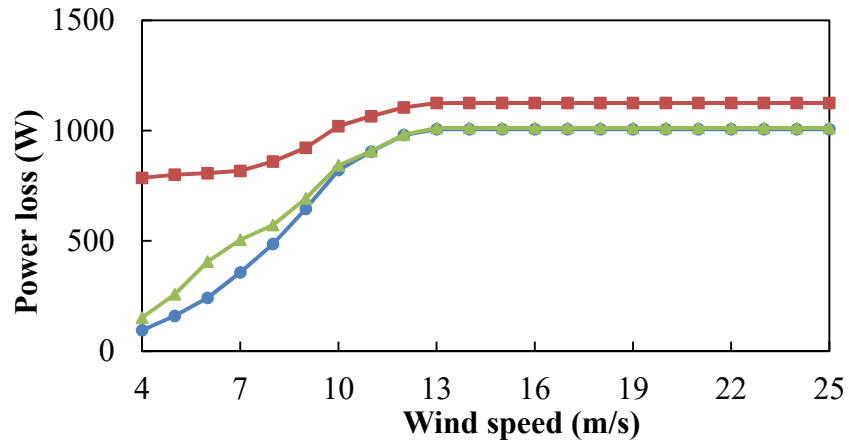
Fig. 2.6. Comparison of power losses of NPC inverter semiconductor devices at the extreme operating condition for different operating modes.



(a)



(b)



(c)

Fig. 2.7. Estimated power losses with different wind speeds at different operating modes for: a) T_1 , b) T_2 , and c) D_{npc} .

Table 2-2

Basic parameters of the grid-side inverter for the selected case study

Rated power of wind turbine P_{rated}	2050 kW
DC-link voltage V_{dc}	1450 V
Fundamental output current frequency f_l	60 Hz
Cut-in wind speed V_{ci}	4 m/s
Grid voltage (RMS) E_g	690 V
Switching frequency f_s	2 kHz
Grid filter inductance L_f	330 μ H
Cut-off wind speed V_{co}	25 m/s

2.5.2 Thermal Behavior Analysis

The thermal behavior of semiconductor devices is investigated to calculate the operating junction temperature T_j and temperature fluctuations ΔT_j at different operating modes. Research has reported that thermal model can be equalized to two different electrical models: Cauer model [44], and Foster model [45]. Foster model is based on experimental results and therefore it is preferable by industry side. A schematic diagram for thermal modeling of power semiconductor devices is shown in Fig. 2.8. Power semiconductor devices are composed of different layers that represent the thermal impedance of the device in addition to thermal impedances of the thermal integrated material part, and module cooling part. Then, the equivalent Foster model is deduced and its parameters are extracted from components datasheets. Table 2.3 summarizes the thermal parameters of Foster model for the selected case study. The operating ambient temperature T_a of the inverter is determined to be equal to 50 °C during the case study. The junction temperature of power semiconductor devices T_j and temperature fluctuation ΔT_j can be calculated as follows:

$$T_{j,T/D} = T_a + P_{loss,T/D} \cdot \sum_{i=1}^4 R_{th(j-c)T/D(i)} + (P_{loss,T} + P_{loss,D}) \cdot (R_{th(c-h)} + R_{th(h-a)}) \quad (2.7)$$

$$\Delta T_{j,T/D} = 2 \cdot P_{loss,T/D} \cdot \sum_{i=1}^4 \frac{R_{th(j-c)T}}{D(i)} \cdot \frac{(1 - e^{-\frac{t_{on}}{\tau_{th(j-c)T/D(i)}}})^2}{1 - e^{-\frac{t_e}{\tau_{th(j-c)T/D(i)}}}} \quad (2.8)$$

where, $P_{loss,T}$, $P_{loss,D}$ are the total power losses through power IGBT, and its freewheeling diode, respectively. $R_{th(j-c)}$ and $R_{th(c-a)}$ represent the Thevenin equivalent thermal resistances between junction and case, and between case and ambient, respectively. The subscripts T and D in (2.7) and (2.8) represent the IGBT and its freewheeling diode, and i represents the layer number of equivalent Foster model of the junction to case impedance. Whereas, t_{on} is the time of ON-state of the power IGBT during the output current fundamental period t_e , and $\tau_{th(j-c)T/D}$ represents the time constant of the Foster layers of module junction to case impedance. In the case of the clamping diode D_{npc} , the junction temperature, and temperature fluctuation are calculated in the same manner as in (2.7) and (2.8) with $P_{loss,T}$ is set to zero.

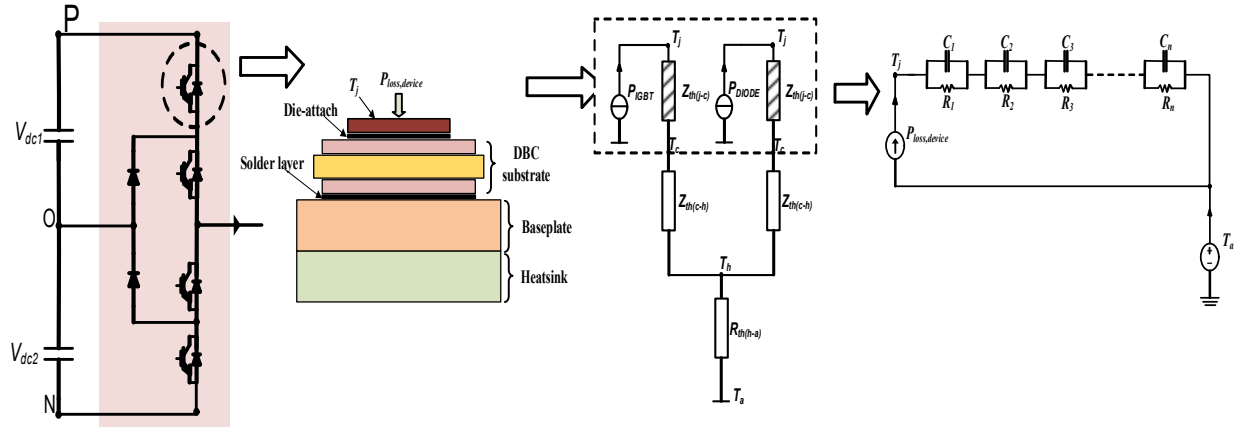


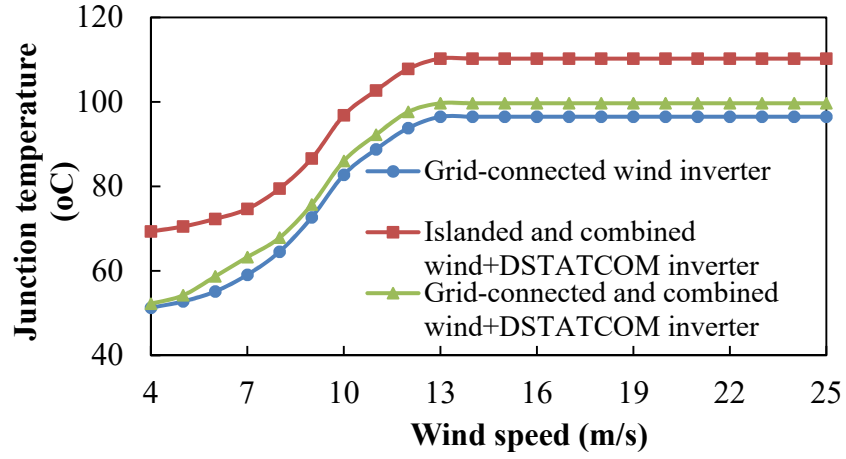
Fig. 2.8. Thermal modeling deduction for different layers in power semiconductor devices of NPC inverter.

This part presents and compares the thermal stresses of semiconductor devices of NPC inverter in resilient microgrid at different operating modes. The thermal stresses are expressed by the calculated junction temperature using (2.7) and temperature fluctuations using (2.8). Fig. 2.9 shows the junction temperature T_j for semiconductor devices T_1 , T_2 , and D_{npc} with different wind speeds at different operating modes. It is clear that the junction temperature T_j of semiconductor devices significantly changes amongst different operating modes and different wind speeds. It is obvious that IGBT devices T_1 , and T_2 have higher junction temperature than other devices in all operating modes. The wind inverter with DSTATCOM functionality in islanded mode represents the extreme operating mode in terms of the thermal loading profiles of semiconductor devices. Temperature fluctuations can be calculated in the same manner.

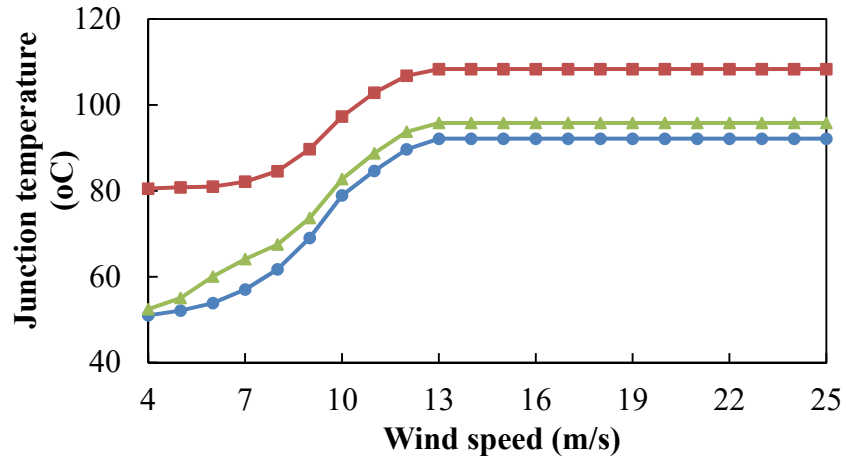
Table 2-3

Thermal model parameters of semiconductor devices.

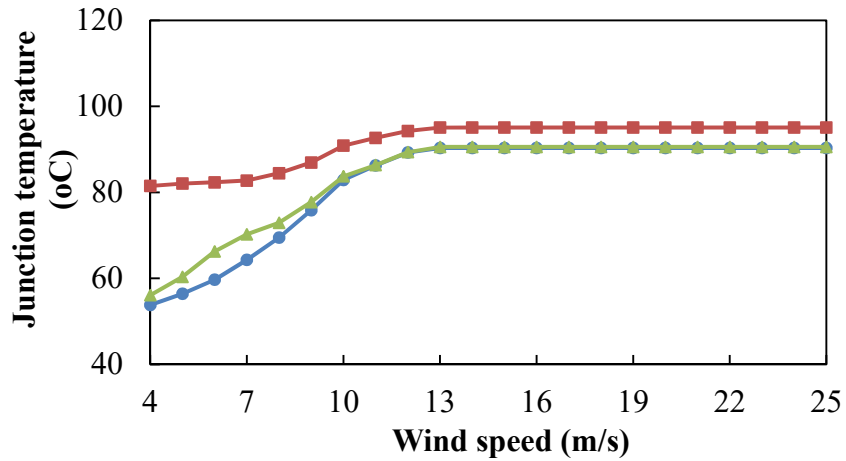
Power module (junction to case)				
Layer number i	1	2	3	4
$R_{th(j-c)T(i)}$ [K/kW]	5.059	1.201	0.495	0.246
$\tau_{th(j-c)T(i)}$ (ms)	202.9	20.3	2.01	0.52
$R_{th(j-c)D(i)}$ [K/kW]	8.432	1.928	0.866	0.839
$\tau_{th(j-c)D(i)}$ (ms)	210	29.6	7.01	1.49
Case to ambient				
$R_{th(c-h)}$ [K/kW]	9	$R_{th(h-a)}$ [K/kW]	10	



(a)



(b)



(c)

Fig. 2.9. Estimated junction temperature ($^{\circ}\text{C}$) at different wind speeds for different operating modes for: a) T_1 , b) T_2 , and c) D_{npc} .

2.6 Lifetime Estimation for Power Semiconductor Devices

This section introduces the analytical calculations and comparisons of lifetime of NPC inverter considering stresses on semiconductor devices due to different operating modes. In [46], a review of several approaches for lifetime estimations of IGBT switches is introduced. A compromise between accuracy and complexity is needed when selecting lifetime assessment model as considering many factors in mathematical representations of lifetime results in extra uneven complexity of the models. Lifetime assessment of power semiconductor devices in this chapter relies on using the Coffin–Manson model for its generality and simplicity. The lifetime expectancy can be expressed as the number of cycles that power semiconductor devices perform effectively. In this model, the number of cycles to failure of semiconductor devices is calculated as [14]:

$$N_f(S_n) = A. (\Delta T_j(S_n))^\alpha. \exp\left(\frac{E_a}{K_b T_j(S_n)}\right) \quad (2.9)$$

From this model, it is clear that number of cycles to failure $N_f(S_n)$ for n^{th} JPDF combination S_n is strongly correlated to the mean junction temperature $T_j(S_n)$ and temperature fluctuations $\Delta T_j(S_n)$ of power semiconductor device at S_n combination. Factors α and A can be obtained from power semiconductor manufacturer tests and power cycling test clarified in [47]. Whereas, E_a represents activation energy and K_b represents Boltzmann constant. The parameters for the lifetime estimation using Coffin-Manson model in (2.9) are listed in Table 2.4.

Different loading profiles including wind power distribution and load demand distribution for different operating modes of NPC inverter in resilient microgrids are essential for comparison of the consumed lifetime per one year of operation. It is assumed that loading

profiles are repetitive every year in the selected case study. The lifetime consumption per one year of operation of power semiconductor devices for each JPDF combination $CL_m(S_n)$ for power semiconductor devices can be calculated as in [48]:

$$CL_m(S_n) = prob(S_n) * \frac{365.25 * 24 * 3600 * f_l}{N_f(S_n)} \quad (2.10)$$

where $prob(S_n)$ is the probability of the n^{th} JPDF with $N_f(S_n)$ number of cycles to failure, f_l is the fundamental frequency of the grid current. Then, the total lifetime consumption per year TCL for different power semiconductor devices can be assessed by composing the consumed lifetime for all JPDF states for each mode using Miner's rule [18] as:

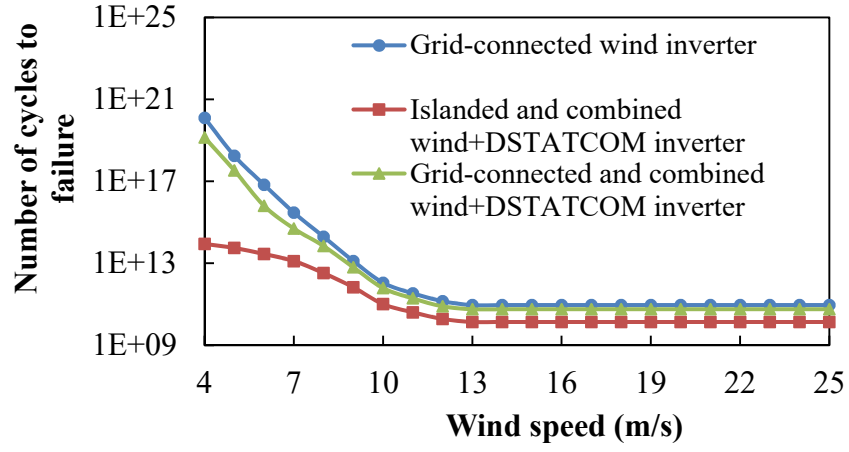
$$TCL = \sum_{S=1}^N CL_m(S_n) \quad (2.11)$$

Based on analytical number of cycles to failure $N_f(S_n)$ in (2.9), the lifetime of semiconductor devices in NPC inverters can be estimated for different operating modes. Fig. 2.10 shows the comparison of N_f for semiconductor devices at extreme operating conditions for different operating modes. It is clear that NPC inverter with DSTATCOM functionality operating in islanded mode has the lowest value for N_f . This is due to that this mode has higher junction temperature and temperature fluctuation values compared to other operating modes. Furthermore, the results show that the IGBT devices T_1 , and T_2 are predicted to have the shortest lifetime in overall operating wind-load combinations and different operating modes as well.

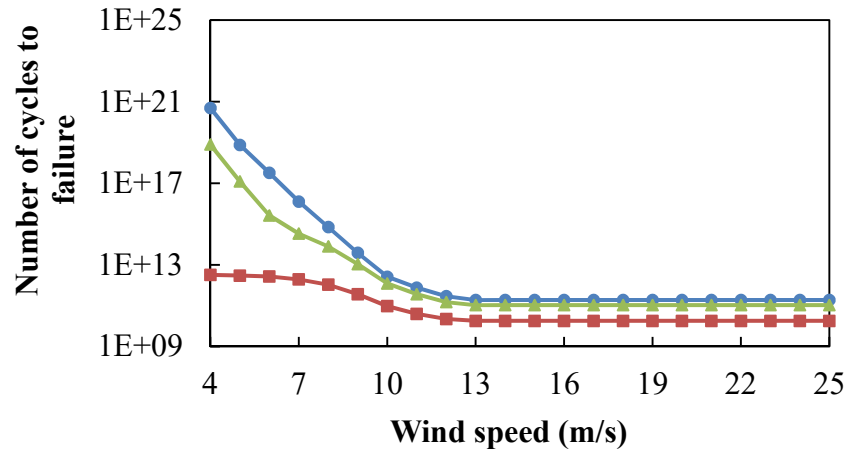
However, the number of cycles to failure N_f cannot be handled alone as the inverter is subjected to different wind-load profiles during operation. The consumed lifetime per one year of operation $CL_m(S_n)$ for power semiconductor devices can be estimated using (2.10)

based on JPDF S_n and the previously estimated number of cycles to failures $N_f(S_n)$. For simplicity of comparison, the consumed lifetime is expressed for each wind speed variation by adding consumed lifetime for combined wind speed and loads demands for that speed. A comparison of total consumed lifetime of power semiconductor components for different operating modes is shown in Fig. 2.11 for power semiconductor devices T_1 , T_2 , and D_{npc} , respectively. The comparison indicates that power IGBTs T_1 , and T_2 have lower lifetime than clamping and freewheeling diodes regardless of the operating mode. Therefore, the lifetime of wind power inverter is defined by corresponding lifetime of power IGBTs. The islanded mode of wind power inverter with DSTATCOM functionality consumes more lifetime per year than other operating modes. This means that the consumed lifetime per 1 year of operation becomes higher with the increased reactive power injection by the inverter.

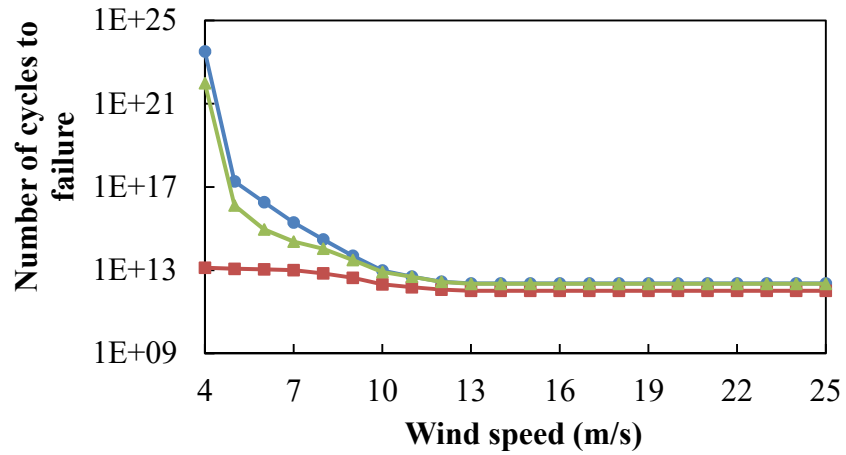
It is worth nothing to express the lifetime of the system by its weakest element. The normalized total consumed lifetime TCL per year of operation is assessed for different operating modes as shown in Fig. 2.12. The grid-connected wind inverter with active power injection has an annual lifetime consumption of $2.16\text{E-}4$, whereas combined wind+DSTATCOM inverter has TCL of $3.63\text{E-}4$ in grid-connected mode and annual TCL of $5.66\text{E-}4$ in islanded mode. This means that operating in resilient microgrid operation results in lowering the lifetime of power inverters 1.68 times with respect to conventional grid-connected wind inverter.



(a)



(b)



(c)

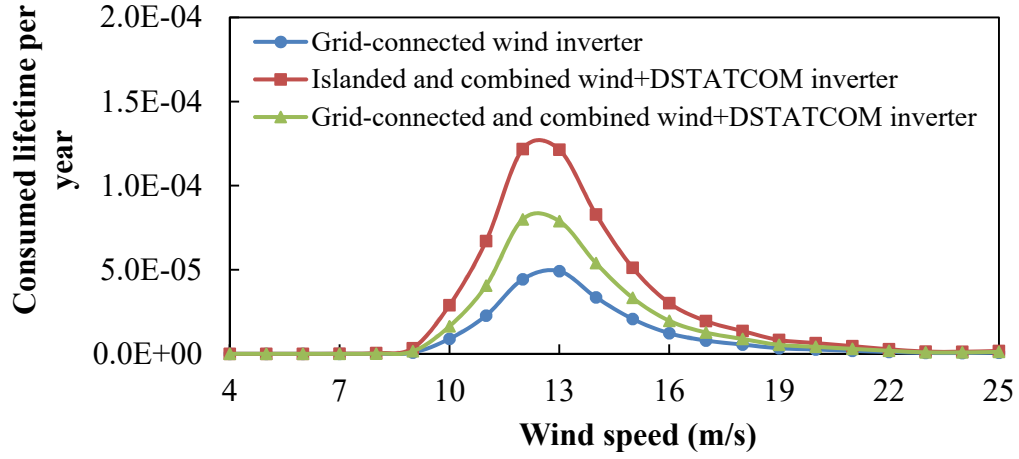
Fig. 2.10. Estimated number of cycles to failures N_f for extreme operating conditions at different operating modes for: a) T_1 , b) T_2 , and c) D_{npc} .

However, resilient microgrid operation involves both grid-connected and islanded modes of operation. Fig. 2.12 shows two cases of hybrid modes of operation with (case I: 50% grid-connected, 50% islanded, and case II: 70% grid-connected, 30% islanded, respectively). The annual TCL has been reduced with hybrid modes of operation and with the change in percentage contribution of each mode compared to the islanded mode of operation. However, compared with using two separate inverters for wind and DSTATCOM functionalities, the combined functionalities inverter has lower initial cost with moderate lifetime consumption during operation. Therefore, the assessment of grid inverters according to consumed lifetime of power devices is highly coveted considering different operating conditions and control methodologies. It can also be included as a part of stochastic planning for new sites of WECS so as to provide precede prediction of failure rates and maintenance requirements.

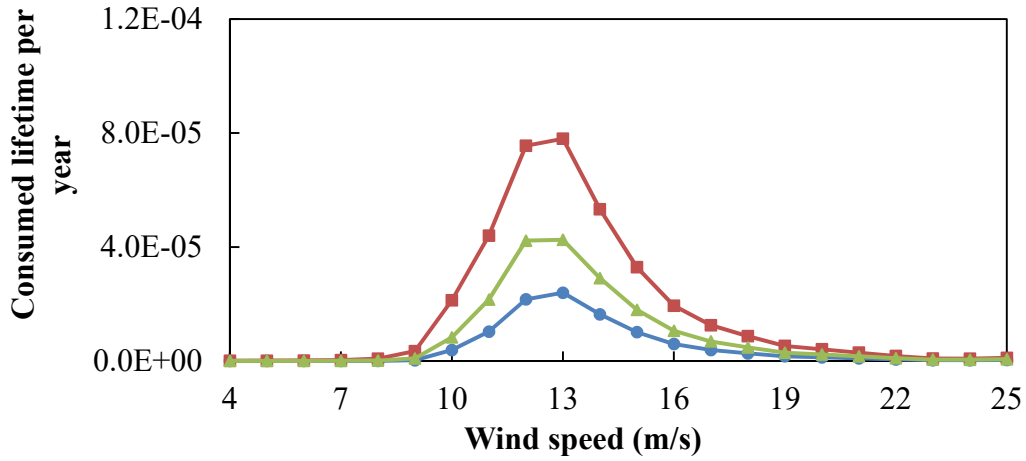
From another side, the utilization factor (UF) of power components gives a measure of the amount of actual apparent power (VA) through power components compared to their maximum VA ratings. The UF can be expressed as follows:

$$UF(\%) = \frac{\text{Total VA.hr output per year}}{\text{Maximum VA ratings} * 8760} * 100\% \quad (2.12)$$

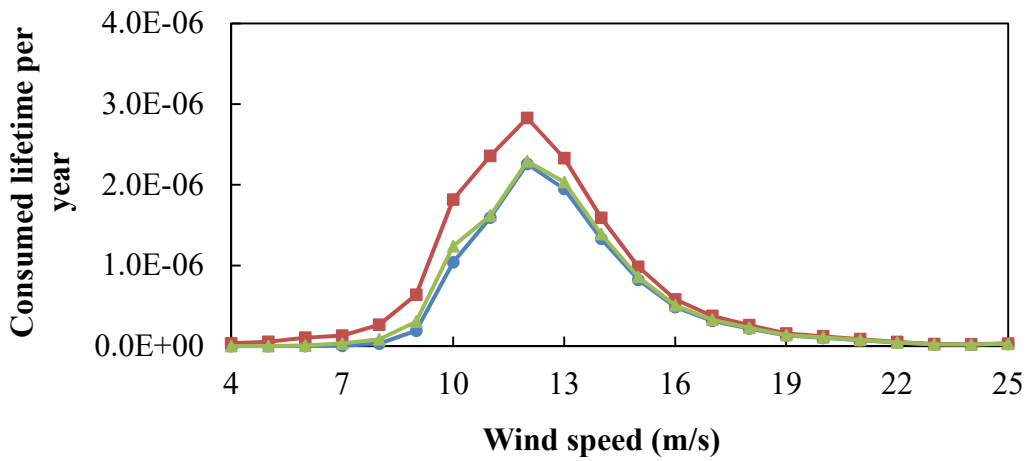
The UFs for different operating modes of NPC inverters in resilient microgrids are listed and compared in Table 2.5. The islanded and combined wind+DSTATCOM inverter represents the highest operating mode for component utilization, whereas grid-connected DSTATCOM inverter represents the lowest mode. Therefore, it can be concluded that the lifetime consumption of power components is directly proportional to their operating UF.



(a)



(b)



(c)

Fig. 2.11. Consumed lifetime per 1 year of operation for different wind speeds at different operating modes for: a) T_1 , b) T_2 , and c) D_{npc} .

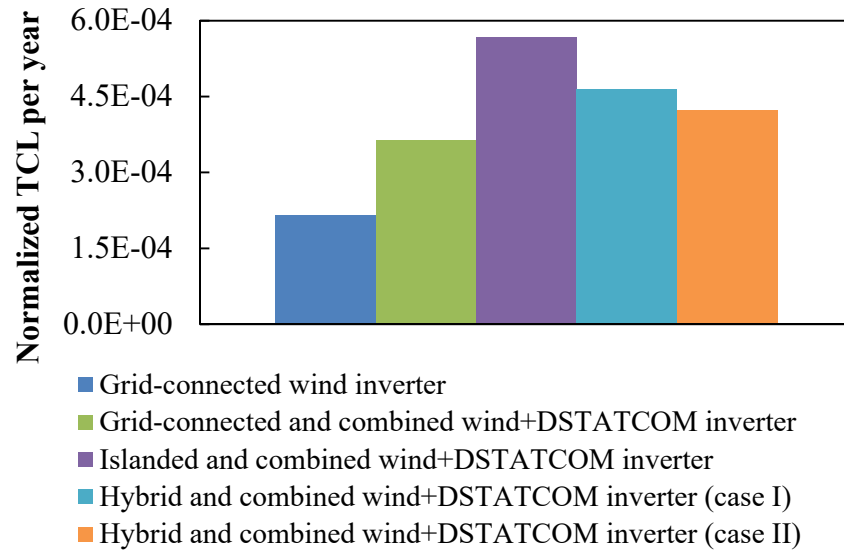


Fig. 2.12. Estimated normalized TCL per 1 year of operation of NPC inverter in resilient microgrids for different operating modes.

Table 2-4

Parameters for the lifetime estimation using Coffin-Manson model.

A	3.03E+05	E_a	9.89E-20
α	-5.039	K_b	1.38E-23

Table 2-5

Comparison of the UF for different operating modes.

Operating mode	Utilization factor (UF)
Grid-connected wind inverter	47.84%
Grid-connected DSTATCOM inverter	36.91%
Grid-connected and combined wind+DSTATCOM inverter	54.94%
Islanded and combined wind+DSTATCOM inverter	63.13%

2.7 Practical Considerations

WECSs are subjected to different operational characteristics including field data properties, available power devices in the market, and operational ratings and demands of the systems. Therefore, practical considerations have to be accounted in order to generalize the proposed approach as follows:

2.7.1. Different Sources and Locations Handling

The proposed approach is generalized and can be applied to different renewable energy sources (RES). The stochastic property is common for various renewable energy sources [49]. In addition, installing RES in various locations results in having different wind profiles and in accordance their loading profiles. Based on the gathered field data of the RES location, the first step of applying the proposed approach is to obtain PDFs of RES and load demand. Afterward, JPDF of the combined RES and load demand is obtained in the same manner as in Section 2.3.4. Then, the same procedures of the proposed approach are applied as in Section 2.4.2.

2.7.2. Wind Speed and Load Demand Uncertainties

Although wind speed profiles and load demand profiles are intermittent and cannot be precisely forecasted [50]. The wind speed and load demand uncertainties can be modeled and incorporated into the proposed approach. Considering wind speed uncertainty level ζ , the wind profile $V_i(t)$ is discretized into three values of $V_i(t) \in \{(1-\zeta)V_i(t), V_i(t), (1+\zeta)V_i(t)\}$ that represent low, medium and high wind profile scenarios, respectively as shown in Fig. 2.13. Afterward, the PDFs of the three wind profile scenarios are extracted for these three values and the proposed approach is applied for each PDF. Then, the total consumed

lifetime of power semiconductor devices is obtained by averaging the resulting lifetime consumptions for the three scenarios. Furthermore, load demand uncertainty with uncertainty level Γ in the load profile $L_j(t)$ can be treated in the same manner by constructing the three load demand profile scenarios $L_j(t) \in \{(1-\Gamma)L_j(t), L_j(t), (1+\Gamma)L_j(t)\}$. Then, the three PDFs of the load demand scenarios are extracted and incorporated in the proposed approach. Moreover, combined uncertainties of wind speed scenarios and load demand scenarios can be considered in the same way and the given procedures in Section 2.4.2 are applied. In this case, there are 9 different scenarios (3×3) and the total consumed lifetime is obtained by averaging the resulting lifetime consumptions of the 9 scenarios.

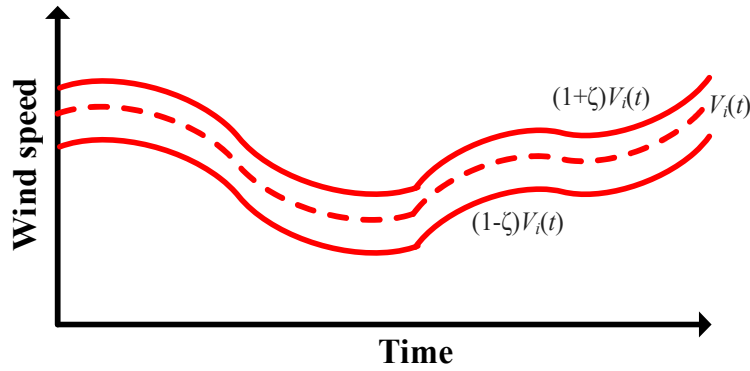


Fig. 2.13. Wind speed profile scenarios due to uncertainty.

2.7.3. Correlation Between Wind Speed and Load Demand Handling

It is assumed in the analysis of the selected case study that wind speed and load demand are not correlated for simplifying the analysis. However, from practical considerations, load demands and wind speeds are correlated, especially in ventilation aspects. In this case, the stochastic dependence between load demand L_j and wind speed V_i is modeled using the well-known copulas, which are often used to model dependency between random variables [37]. More details about the calculations of JPDF in the case of correlation between V_i and

L_j can be found in [49], [51]. Then, the resulting JPDF of wind speed, load demand, and their correlation is used to calculate lifetime consumption in the proposed approach as in Section 2.4.2.

2.7. 4. Configurational Changes

As explained in the introduction Section, WECSs are divided into two main categories: (1) Partial-scale configuration, which is used in DFIG-based WECS, and (2) Full-scale configuration, which is applied to the selected case study using PMSG. In DFIG-based WECSs, loading profiles are obtained using the designed system parameters and the designed amount of partial power through the converters. Additionally, in DFIG-based WECS, both of the rotor side converter and grid side converter are capable of injecting reactive power into the grid. All these factors with percentage shares of both converters are combined in order to define the loading profiles of the system components. Then, thermal stresses and lifetime consumption assessment procedures are proceeded by the proposed approach.

2.7. 5. Different Operating Ratings

The most important factors that being altered for different WECS are the loading profiles and the datasheet parameters of the selected power electronic devices. Therefore, constructing the loading profiles including P_w and Q_s of the system using (2.3) and (2.4) represents the first step for various systems with different operating ratings. Then, loss and lifetime models are constructed for the selected devices for the system ratings using their manufacturers' datasheets. Afterward, the proposed approach is applied to assess thermal stresses and lifetime consumption for the desired system.

2.7. 6. Capabilities and Constraints of WECS

WECSs components and controls are subjected to various constraints in order to increase their lifetime and their economic operation. The reactive power capabilities of individual WECS are subjected to the following constraints:

$$Q_{s,max} = \sqrt{S_{inv}^2 - P_w^2} \quad (2.13)$$

where, $Q_{s,max}$ represents the maximum allowable reactive power of the inverter at active power injection of P_w and S_{inv} represents the apparent power rating of the inverter. Moreover, the thermal stresses of the operating point of power semiconductor devices are constrained by their maximum allowable junction temperature $T_{j,max}$, which is expressed as follows:

$$T_j = < T_{j,max} \quad (2.14)$$

Power semiconductor devices manufacturers provide the values of $T_{j,max}$ in their datasheets. Furthermore, the failure criteria of the inverter is constrained by their TCL per year multiplied by the number of years of operation, which can be expressed as follow:

$$TCL * No\ of\ years < 1 \quad (2.15)$$

In wind farm operation with z wind turbines, the control is constrained by:

$$0 \leq Q_{s,i} \leq Q_{s,max,i} \quad (2.16)$$

$$E_{t,min} \leq E_{t,i} \leq E_{t,max} \quad (2.17)$$

$$\sum_{i=1}^z Q_{s,i} - Q_{loss} = Q_{WF} \quad (2.18)$$

where, $Q_{s,i}$, and $E_{t,i}$ represent the reactive power injection and the terminal voltage of the i^{th} wind turbine. $Q_{s,max,i}$ represents the maximum reactive power injection of the i^{th} wind turbine. $E_{t,min}$, $E_{t,max}$ represent the up and down terminal voltage limits of the wind turbine. Whereas Q_{WF} , Q_{loss} represent the total reactive power injection by the wind farm, and the reactive power losses, respectively.

2.7. 7. Various Networks Integration

With the increased number of renewable energy sources (RESs), the active distribution network (ADN) represents a wider framework for modeling, management, and scheduling of various RESs [52]. Moreover, ADNs can manage different RESs in a more economic and a more reliable manner. The proposed approach can be incorporated into ADNs and can enhance their management and reliability performance by: (1) Predicting thermal stresses of injected active and reactive powers on different system components, (2) Providing measures of the remaining useful lifetime of power components for maintenance and for new installation plans, and (3) Providing easier framework for resiliency and sectionalization of ADNs at emergency conditions.

2.8 Conclusions

A powerful approach for thermal behavior, and lifetime assessment for WECSs that reflect the influence of the added DSTATCOM functionality, and various modes of resilient microgrids operation has been proposed in this chapter. The proposed approach has three sequential steps: (1) the loading profiles of different operating modes of the inverter are transformed into electrical loading profiles on semiconductor devices, (2) Analytical estimations of power losses and thermal behavior based on datasheets available from

manufacturers are used to determine and to compare the most stressed components of the system. Then, the lifetime consumption can be assessed and compared at different operating modes of NPC inverter in resilient microgrids using Coffin-Manson lifetime models, and (3) Annual lifetime consumption can be estimated and compared based on Miner rule and by using wind-load JPDF for different operating modes.

The proposed approach has demonstrated that wind inverter with DSTATCOM functionality in the islanded mode of operation represents the extreme operating mode in terms of thermal loading profiles of semiconductor devices. Additionally, adding DSTATCOM functionality to grid-connected WECS has resulted in 1.68 lower lifetime than in normal WECS operation with only active power injection in the selected case study. Although adding more functionalities reduces the initial cost of the system and better utilization of the components.

By applying the proposed approach, more precise estimations of thermal stresses and lifetime consumption have been obtained with considering the stochastic behaviors of wind power and load demands in addition to operational characteristics of resilient microgrids. In addition, the proposed approach provides a straightforward environment for planning and control engineers, in accordance to these evaluations, in order to properly select suitable power components, revalue the added functionalities, and develop new control methodologies.

Chapter 3

Thermal Stresses Relief Carrier-Based PWM Strategy for Single Phase Multilevel Inverters

3.1 Overview

Enhancing power cycling capability of power semiconductor devices is highly demanded in order to increase the long term reliability of multilevel inverters. Ageing of power switches and their cooling systems leads to their accelerated damage due to excess power losses and junction temperatures. Therefore, thermal stresses relief (TSR) is the most effective solution for lifetime extension of power semiconductor devices. This chapter presents a new thermal stresses relief carrier-based pulse width modulation (TSRPWM) strategy for extending the lifetime of semiconductor switches in single-phase multilevel inverters. The proposed strategy benefits the inherent redundancy among switching states in multilevel inverters to optimally relieve the thermally stressed device. The proposed algorithm maintains the inverter operation without increased stresses on healthy switches and without reduction of the output power ratings. In addition, the proposed algorithm preserves voltage balance of the DC-link capacitors. The proposed strategy is validated on single phase five level T-type inverter system with considering different locations of thermal stresses detection. Experimental prototype of the selected case study is built to verify the results. Moreover, comparisons with the most featured strategies in literature are given in detail.

3.2 Introduction

3.2.1 Single Phase T-Type Multilevel Inverters

Power electronic converters play an important role in several applications for power generation, storage, delivery and utilization as they acquire higher efficiency and performance. However, power electronics have evinced high failure rates among system components that put their reliability enhancement and lifetime prolongation of major concerns [53]. Power semiconductor devices represent one of the critical elements that define the overall system reliability and robustness [16]. According to [54], thermal stresses including high junction temperature and large junction temperature cycling are the prime root causes of semiconductor failures. In regards, several studies have been performed on reliability of semiconductor devices related to thermal stresses such as failure mechanisms, lifetime models, and thermal management techniques [7].

A generalized diagram of n -level full bridge T-type single phase inverters is shown in Fig. 3.1. For any n -level T-type inverter, there are $n-3$ DC-link capacitors that create different output voltage levels. Then, power semiconductor devices are controlled to output these voltage levels to the load. Power semiconductor devices are usually subjected to continuous dynamic loading that results from power and temperature cycling. These repeated loading in addition to the large mismatch of coefficients of thermal expansion (CTE) of power semiconductor layers cause thermo-mechanical fatigue in the form of bond wires lifting off and solder delamination [55]. These ageing effects of power semiconductor devices gradually increase the equivalent thermal resistance of the device, which is reported at failure to be about 20% above its normal value. Then increased thermal stresses are expected that fasten the failure of the device. In addition, ageing of the forced cooling

system of power semiconductor devices can lead to the same effects. Therefore, thermal stresses relief (TSR) of semiconductor devices is highly required if increased thermal stresses have been detected in one of the power semiconductor devices.

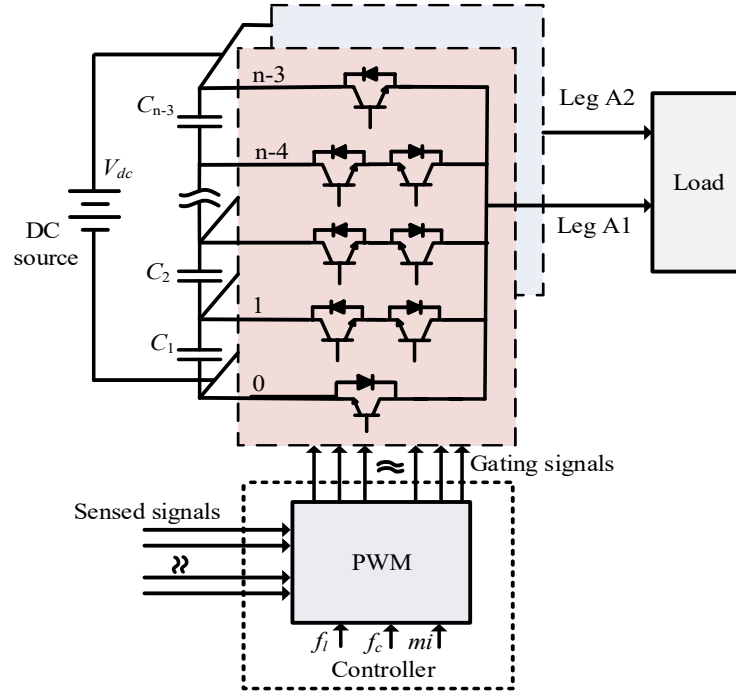


Fig. 3.1. A schematic diagram of PWM controlled full bridge n -level T-type inverter.

3.2.2 Existing Issues in Thermal Management Methods

Several strategies of thermal stresses management and relief are provided in literature [6]–[17]. Most of existing conventional strategies rely on derating of the output power [56] or using costly cooling systems [57]. When the operating junction temperature of the semiconductor device exceeds the predefined safety limit, the reference output current of the inverter is reduced and the power losses through the affected device is reduced as a result [56]. A similar strategy for reliability improvement of PV inverters through limiting their maximum feed power is introduced in [58]. However, in this technique, the tested inverter is not operated with its full scale output power and the maximum power point

(MPP) cannot be tracked efficiently in renewable energy applications. On another side, the junction temperature of semiconductor devices can be reduced by adding an additional forced cooling device between the thermal grease of the device and the heatsink [57]. However, the added devices increase the system cost and volume. Further, additional power is required to operate the cooling device. Therefore, cost effective thermal stress relief methods for power semiconductor devices is highly needed in order to minimize the wasted energy due to derating of the inverter and the costly added cooling devices.

Another alternative method for thermal stresses relief of power semiconductor devices is based on optimum design of modulation techniques of inverters. The pulse width of power switches in interleaved converters is controlled to achieve balanced thermal stresses on IGBT devices through percentage share of different interleaved modules [47]. However, full scale components are needed for each interleaved module that increase dramatically the total system cost in these methods.

The redundancies between the switching states of multilevel inverters represent another cost effective solutions for thermal management of IGBT devices [59]. Nevertheless, conventional neutral point clamped (NPC) inverters suffer from unequal loss distribution among devices. Loss redistribution modulation techniques are developed to address this problem [60]. Additionally, the active NPC inverters with modified modulation techniques are developed to achieve losses and stresses reductions [60], [61]. However, the cost and the number of IGBTs in active NPC inverters are high compared to conventional ones. Discontinuous pulse width modulation (DPWM) techniques have been developed in literature to improve the total efficiency of multilevel inverters by reducing switching transitions of semiconductor devices [62], [63]. A DPWM method for power cycling

reliability improvement in NPC inverters is presented in [62]. However, these modulation techniques cannot effectively provide thermal stresses relief for a particular semiconductor device if increased thermal stresses have been detected. Furthermore, DPWM techniques provide dissimilar thermal stresses on different system components.

The same concept with the same features is applied on space vector pulse width modulation (SVPWM) method that is featured with more flexibility [64]. A higher efficiency discontinuous SVPWM method is achieved through avoiding switching the leg with the highest current [64]. Another SVPWM methods for lifetime extension of thermally-overheated semiconductor devices are developed in [65], [66]. These methods provide thermal relief for a particular semiconductor device without compromise of the inverter output ratings. However, additional voltages stresses on power components are introduced to achieve voltage balance over the DC-link capacitors. Moreover, the complexity of calculations and implementation of SVPWM techniques increases at higher number of levels in order to define the operating region and to calculate the dwelling times of voltage vectors.

3.2.3 Contribution

Stimulated by the above-mentioned issues, a new carrier based thermal stresses relief PWM (TSRPWM) strategy is proposed in this chapter in order to alleviate thermally stressed semiconductor devices in single phase multilevel inverters. The proposed algorithm provides the benefits of: simple implementation without increased complexity at higher number of levels; no need for output ratings compromise; cheap solution without extra system cost. In addition, the proposed strategy ensures high performance regarding voltage balance of DC-link capacitors of the multilevel inverter.

This chapter is organized as follows: Section 3.3 explains the principles of thermal stress relief and lifetime extension of power devices. Section 3.4 presents the operation of single phase five level inverters. Section 3.5 provides in details the proposed TSRPWM strategy and its generalized implementation. The feasibility and simulation results of the proposed TSRPWM strategy are investigated on five-level T-type inverter system in Section 3.6. The experimental prototype validation of the proposed strategy are given in Section 3.7. Section 3.8 provides performance criteria comparison of the proposed TSRPWM strategy with the most featured methods in the literature. The conclusions are summarized in Section 3.9.

3.3 Thermal Stresses and Lifetime Extension

Several modulation techniques can be used to drive multilevel inverters, wherein power semiconductor devices are subjected to different conduction times and switching transitions for each particular modulation technique. Fig. 3.2(a) shows the relationship between different models of semiconductor devices and modulation techniques. For the sake of accurate modelling for power losses P_{loss} through semiconductor devices, datasheet based losses calculation methods are mostly preferred and the method in [43] is used in the chapter. Then, using thermal models of semiconductor devices, the operating junction temperature T_j and junction temperature cycling ΔT_j can be obtained for the device as in (3.1) and (3.2) [14]:

$$T_j = T_h + P_{loss} \cdot \sum_{i=1}^4 R_{th(i)} + P_{loss} \cdot R_{th(c-h)} \quad (3.1)$$

$$\Delta T_j = 2 \cdot P_{loss} \cdot \sum_{i=1}^4 R_{th(i)} \cdot \frac{(1 - e^{-\frac{t_{on}}{\tau_{th(i)}}})^2}{1 - e^{-\frac{t_e}{\tau_{th(i)}}}} \quad (3.2)$$

where, T_h denotes to the operating heatsink temperature in Celsius, and $R_{th(i)}$ and $\tau_{th(i)}$ represent the thermal resistances and thermal time constant for i^{th} layer of the thermal model between the junction and case of semiconductor device. $R_{th(c-h)}$ represents the thermal resistance between case and heatsink of the device. Whereas t_{on} is the time of on-state of the power IGBT during the output current fundamental period t_e .

The number of cycles to failure N_f represents a good measure for estimating the expected lifetime for semiconductor devices and can be modelled by the well-known Coffin-Manson model as follows in (3.3) [14]:

$$N_f = A. (\Delta T_j)^\alpha. \exp\left(\frac{E_a}{K_b T_j}\right) \quad (3.3)$$

where α and A are constants that can be obtained from power cycling tests, E_a represents activation energy and K_b represents Boltzmann constant. From (3.1), the main factors that affect the lifetime of semiconductor devices are the thermal stresses over the device (T_j and ΔT_j), which are mainly affected by the power losses through the device on-state duration of the output current of the inverter. The effect of thermal stress relief on the lifetime of semiconductor devices is shown in Fig. 3.2(b) [67]. It is found that a small decrease of thermal stresses leads to a great enhancement of the semiconductor device lifetime.

Fig. 3.3 shows a schematic diagram of a complete thermal relief system for IGBT device S_{Axy} (where x denotes to leg number 1, or 2, and y denotes the switch location 1, 2, ... in the leg) in the multilevel inverter. The thermal stresses relief (TSR) system for power semiconductor devices has three main steps:

- 1) Estimating thermal stresses using thermo-sensitive electrical parameters (TSEP) [68] for obtaining T_j and ΔT_j of the device;
- 2) Applying thermal stresses detection (TSD) algorithm of the device;
- 3) Activating thermal stresses relief (TSR) algorithm.

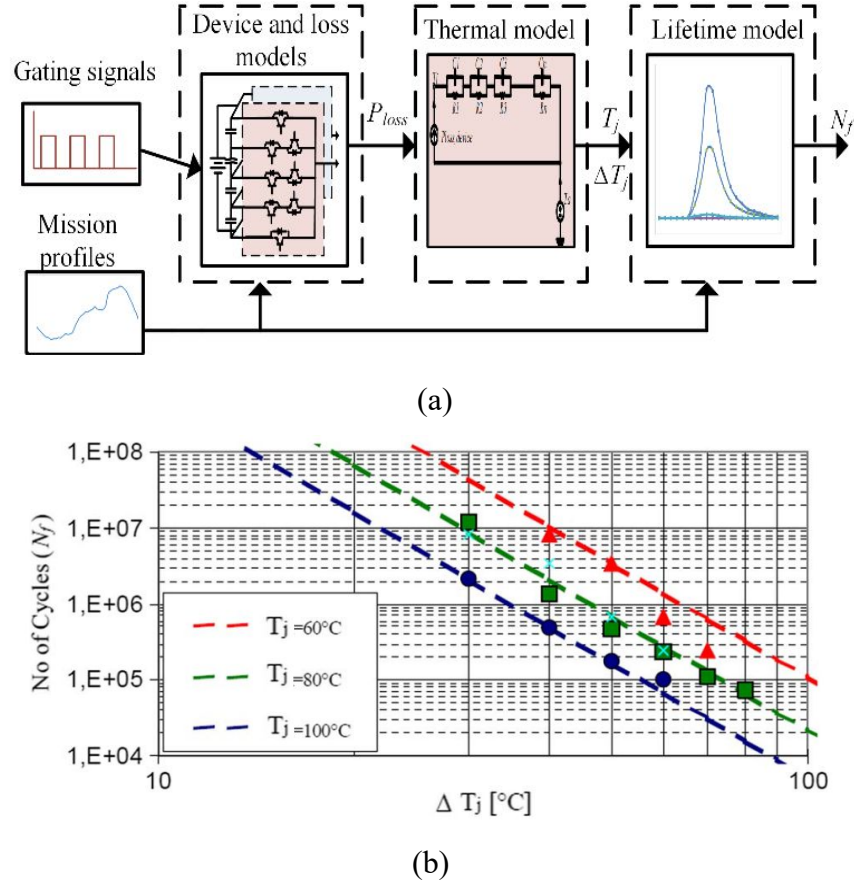


Fig. 3.2. Various models of power semiconductor device: (a) Relationship between models, and (b) N_f versus T_j and ΔT_j [20].

The recently developed thermo-sensitive electrical parameters (TSEP) methods present a good solution to estimate the thermal stresses of semiconductor devices. Then, the estimated T_j and ΔT_j are fed to TSD system that compares the estimated T_j and ΔT_j with the maximum operating thermal stresses ($T_{j,limit}$, and $\Delta T_{j,limit}$), which are provided by devices' manufacturers. Finally, a flag representing thermal stresses relief enable ($TSR_en(S_{Axy})$) signal is fed to the TSR algorithm to alleviate the thermal stresses of the affected device S_{Axy} , where $TSR_en(S_{Axy})$ equals to 1 if TSR is required and 0 otherwise. In this chapter, the problem of the increased thermal stresses detection (TSD) has not been tackled. Additionally, it is emulated and implemented by an external ON/OFF switch.

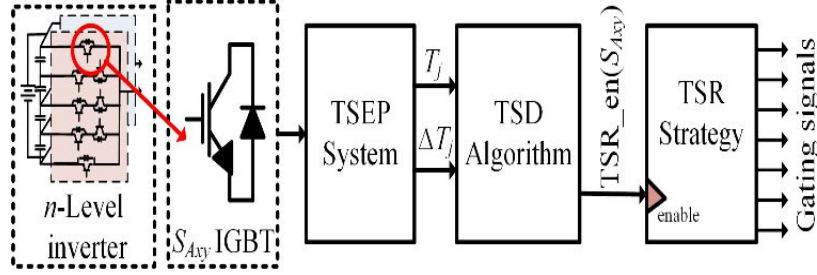


Fig. 3.3. Schematic diagram of the thermal stresses relief (TSR) system.

3.4 Single Phase Five Level Inverter Operation

Fig. 3.4 shows the power stage of single phase five level T-type inverter. Two equal DC-link capacitors are used to generate the voltage levels, which are connected to the load through the IGBT switches. Each leg of the inverter can generate either V_{dc1} , 0, or $-V_{dc2}$ with respect to neutral point O by connecting the output to the inverter's points P, O, or N, respectively. Therefore, the two legs of the inverter are combined to generate five levels at the output of the inverter that are $+(V_{dc1} + V_{dc2})$, $+V_{dc1}$, 0, $-V_{dc2}$, and $-(V_{dc1} + V_{dc2})$. The controller is required to maintain voltage balance of the two DC-link capacitors ($V_{dc1} = V_{dc2} = 0.5V_{dc}$), and the output levels at this case will be $(+V_{dc}, +0.5V_{dc}, 0, -0.5V_{dc}, \text{ and } -V_{dc})$.

The modulation technique is employed to generate various levels of the inverter output voltage. Most common technique is the level shifted PWM modulation [69], where $n-1$ carriers are needed to generate n -levels at the output. The modulating signal and the carrier signals for five-level inverters are shown in Fig. 3.5. The gating signals for the IGBT switches are generated by continual comparison of the modulating signal V_m with the four carrier signals $V_{cr1}-V_{cr4}$. According to the amplitude and polarity of the modulating signal V_m , the line period of V_m is divided into six operating regions R1-R6 as clarified in Fig. 3.5. Two different voltage levels are generated in each region. Fig. 3.6 shows the generated

voltage levels at each region R1-R6 of the inverter output. For instance, the voltage levels 0, and $0.5V_{dc}$ are generated in region R1 with dwelling times of t_1 and t_2 , respectively.

Table 3.1 summarizes inverter switching combinations with their effects on the voltages of DC-link capacitors for generating the output levels of the inverter (where $\uparrow$ represents charging mode, $\downarrow$ represents discharging mode, and $-$ represents no effects on capacitor voltages). It is clear from Table I that each of $+0.5V_{dc}$, and $-0.5V_{dc}$ voltage levels can be implemented by using two different paths with different switch combinations and different effects on the voltages of DC-link capacitors. Moreover, there are three different paths to implement zero voltage level. Therefore, there are a degree of freedom to select different switches and capacitors combinations to synthesize the output voltage levels, and of course extra freedom can be obtained at higher n -levels inverters. This redundancy property can be utilized to enhance the performance of multilevel inverters. The optimum selection of the redundant states is employed to achieve different objectives such as voltage balance of DC-link capacitors, reduction of THD in the outputs, reducing switching power losses, fault tolerant operation, etc.

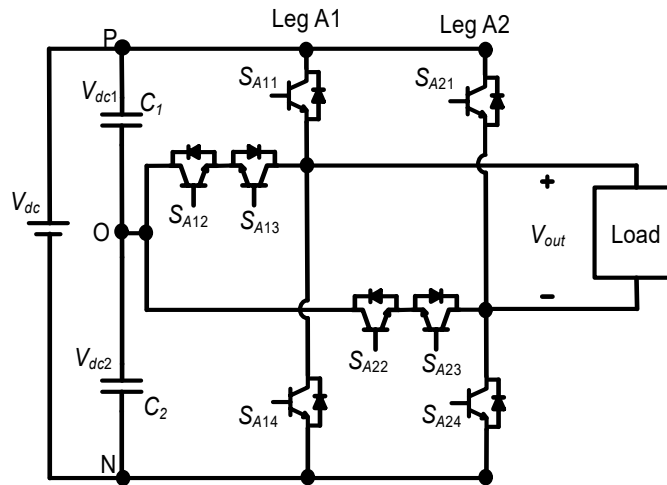


Fig. 3.4. Single phase full bridge T-type inverter system.

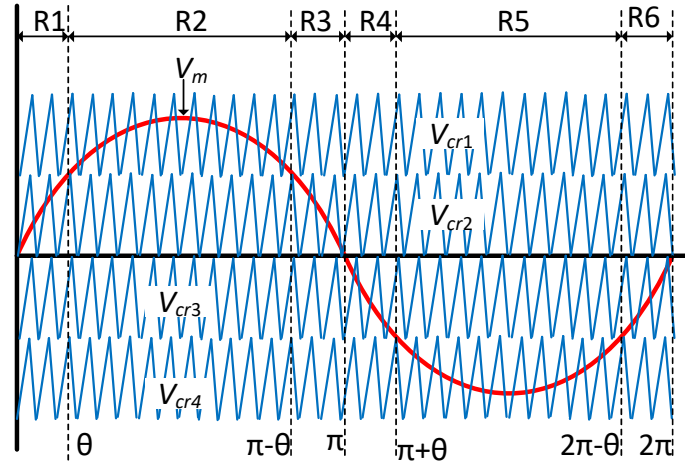


Fig. 3.5. Carrier-based PWM for single phase five level inverters.

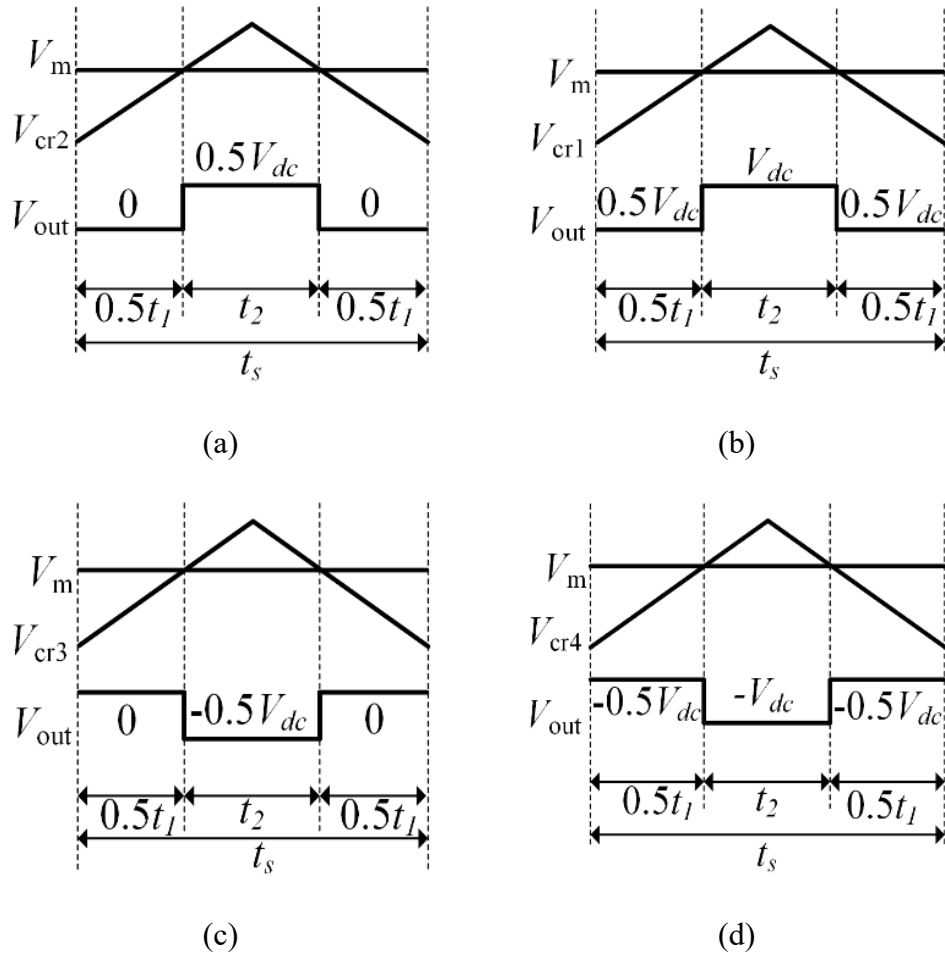


Fig. 3.6. Output voltages of the inverter at regions: (a) R1 and R3, (b) R2, (c) R4 and R6, and (d) R5.

Table 3-1
Switch combinations for different levels of five level inverter

Amp.	S_{A11}	S_{A12}	S_{A13}	S_{A14}	S_{A21}	S_{A22}	S_{A23}	S_{A24}	V_{dc1}	V_{dc2}
V_{dc}	1	0	0	0	0	0	0	1	—	—
$0.5V_{dc}$	1	0	0	0	0	1	1	0	↓	↑
	0	1	1	0	0	0	0	1	↑	↓
0	1	0	0	0	1	0	0	0	—	—
	0	0	0	1	0	0	0	1		
	0	1	1	0	0	1	1	0		
$-0.5V_{dc}$	0	1	1	0	1	0	0	0	↓	↑
	0	0	0	1	0	1	1	0	↑	↓
$-V_{dc}$	0	0	0	1	1	0	0	0	—	—

3.5 The Proposed Strategy

The aforementioned analysis of the redundancy property in multilevel inverters shows the following degrees of freedom to optimize their performance: 1) thermal stress relief of IGBT switches can be obtained by redistributing their power losses through proper selection of redundant switching states; 2) the charge of DC-link capacitors can be balanced by appropriately selecting the charge/discharge switching states. Accordingly, this chapter proposes a new lifetime extension method for alleviating thermally stressed semiconductor devices in multilevel inverters. The proposed thermal stress relief PWM (TSRPWM) strategy is based on carrier based PWM method.

The proposed TSRPWM method can be explained as follows: taking region R2 as an example and according to the required voltage levels in region R2 as in Fig. 3.6(b) in addition to their required switch combinations as in Table 3.1, there are two different switching sequences in this region due to the existence of two different paths to generate $0.5V_{dc}$ voltage level. Fig. 3.7 shows the gating pulses for the two allowable switching

sequences, called S_{eq1} , and S_{eq2} in region R2. It can be observed that different gating pulses are applied in each sequence. For example, S_{A11} is held on in S_{eq1} for the switching period t_s , and it is subjected to only conduction losses as a result. Whereas in S_{eq2} , it is switched on for period t_2 and turned off for period t_1 . Consequently, S_{A11} is subjected to conduction losses during period t_2 and switching losses due to on/off transitions. However, the total power losses varies with different locations of the modulating signal V_m in line period and with different modulation indices mi as well. The same analysis and observations can be done for other switches and for other operating regions. In region R1, there are six switching sequences can be obtained for synthesizing V_m , and different switch pulses are applied for each switching sequence.

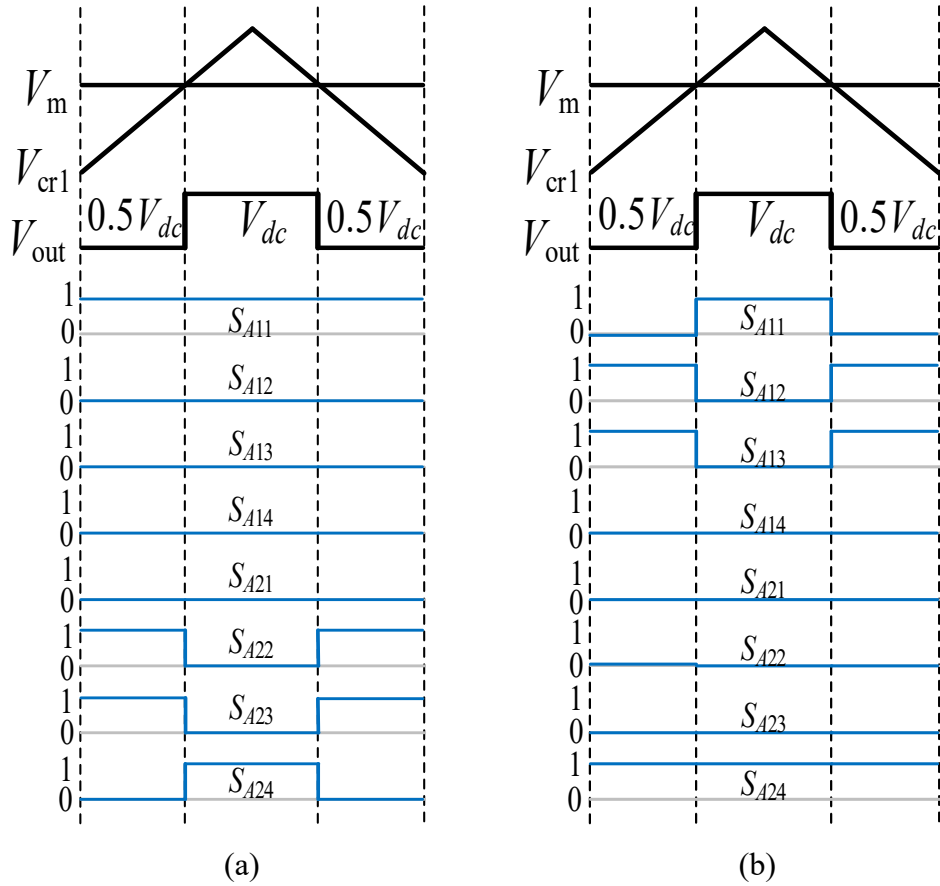


Fig. 3.7. Gating pulses for IGBT switches in region R2 at: (a) S_{eq1} , and (b) S_{eq2} .

Therefore, if an increase of the thermal stresses in one of the IGBT devices S_{Axy} has been detected ($\text{TSR_en}(S_{Axy})=1$), the proposed TSRPWM strategy is applied. Fig. 3.8 shows a generalized flowchart for implementing the proposed TSRPWM strategy for n -level inverter. Firstly, the modulating signal V_m is generated using the required modulation index (mi), and line frequency f_l . While, $n-1$ carrier signals V_{cr} are generated using the number of levels n and the desired switching carrier frequency f_c of the inverter. Secondly, the amplitude and sign of V_m define the current operating region R. The desired output voltage levels is performed by comparing the modulating signal V_m with the $n-1$ carriers V_{cr} . Thirdly, the proposed algorithm checks if there are any TSD in the IGBT switches (if $\text{TSR_en}(S_{Axy})=1$). Lastly, the proposed algorithm has to properly select the redundant switching states that achieve the desired performance and the operating mode of the inverter as it is explained in the following parts.

The inverter has two modes of operation under the proposed strategy namely: 1) normal mode (NORM mode) of operation (if $\text{TSR_en}(S_{Axy})=0$); 2) thermal stress relief mode (TSR mode) of operation (if $\text{TSR_en}(S_{Axy})=1$). In NORM mode, the redundant switching states are selected so as to achieve voltage balance of DC-link capacitors. If $V_{dc1} > V_{dc2}$, the switching states of C_1 discharge are applied. In contrast, if $V_{dc2} > V_{dc1}$, the switching states that discharge C_2 are applied. In case of thermal overstress detection TSD in one of the IGBT devices (TSR mode), the proposed algorithm defines the m valid switching sequences in the current operating region R in the same way as the aforementioned sequences in region R2. Afterwards, a cost function of the power losses $P_{loss}(S_{Axy})$ for the stressed IGBT device is implemented for all valid m switching combinations. This calculations of P_{loss} can be implemented in parallel in FPGA implementation in order to

reduce the required execution time at higher n -level inverters due to the increased number of redundant states. Lastly, the optimizer selects the optimum switching combination of voltage levels that has the minimum power losses through the thermally stressed device. In other regions of the line period that do not utilize the affected device, the optimum switching sequence for achieving voltage balance of DC-link capacitors is selected.

The selected redundant switching states can provide thermal stresses relief to the thermally-stressed IGBT devices and balance the voltages of DC-link capacitors in the same line period. It can be realized from the implementation of the proposed TSRPWM strategy in Fig. 3.8, its procedures are very easy and simple for hardware implantation compared to the complex calculations in SVPWM techniques in [65], [66]. Moreover, the proposed TSRPWM can achieve strong alleviation for the affected device by optimally selecting the redundant switching states. The proposed strategy employs the redundant switching states and hence it can preserve the same output ratings, the same number of output levels, and the same output performance. In addition, the proposed strategy maintains the voltage balance over the DC-link capacitors. The proposed TSRPWM method can be applied to different inverter configurations and topologies.

3.6 Simulation Results

To verify the performance and the effectiveness of the proposed TSRPWM strategy, simulation case study has been implemented in PSIM environment. The simulation study demonstrates the ability of the proposed method to extend the lifetime of thermally-stressed devices, while maintaining voltage balance of DC-link capacitors and same output ratings.

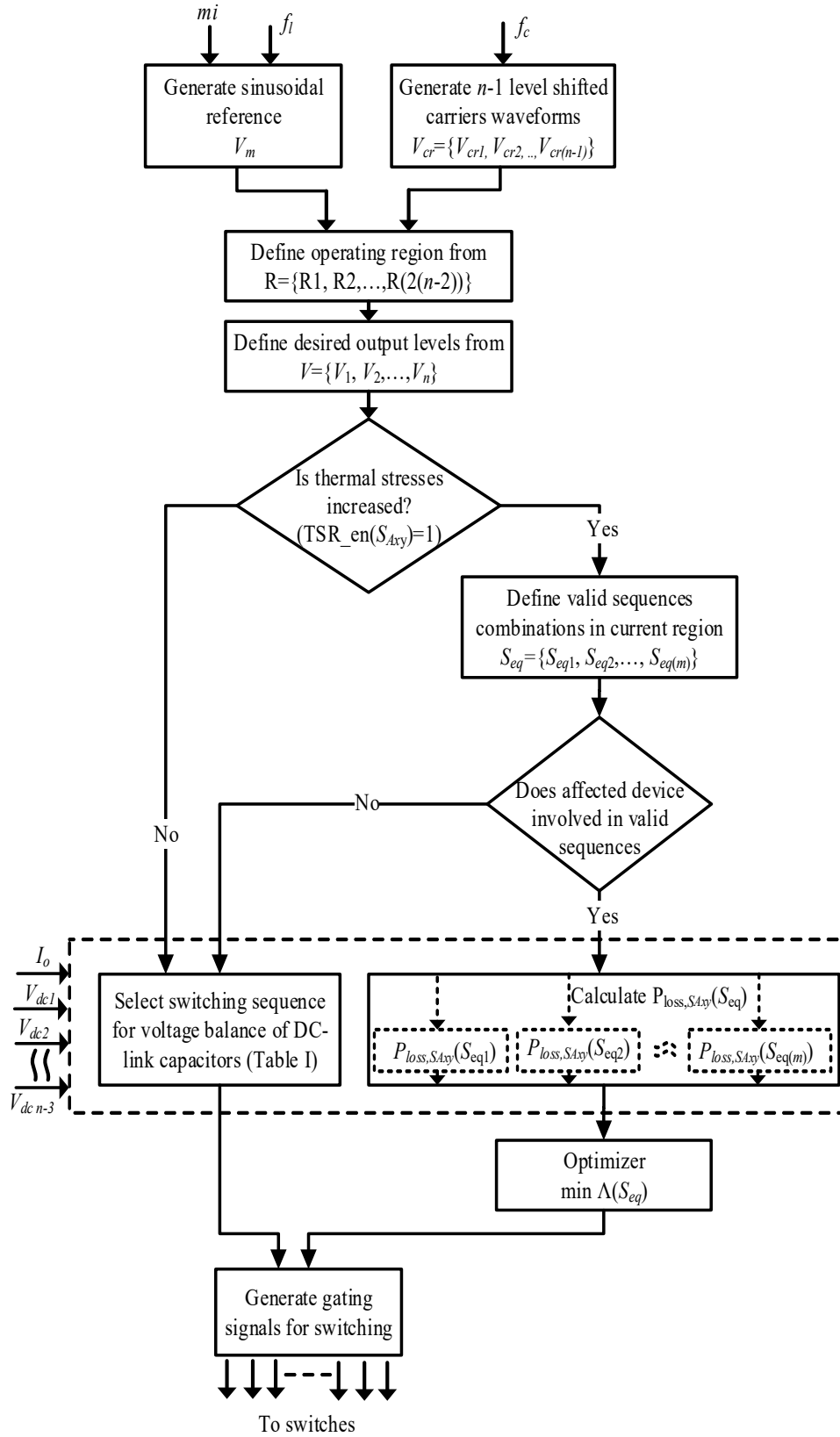


Fig. 3.8. Generalized implementation of the proposed strategy.

The parameters for the simulation studies are listed in Table 3.2. The performance the proposed PWM strategy have been studied during operation in normal mode (NORM mode) and in thermal stresses relief mode (TSR mode). Two different case studies of increased thermal stresses detection (TSD) are considered in IGBTs S_{A11} , and S_{A12} in leg A1 to evaluate the performance of the proposed strategy with different locations of TSD.

In the first case study, it is assumed that there are a TSD in S_{A11} of the inverter ($\text{TSR_en}(S_{A11})=1$) at time 0.25 seconds. Fig. 3.9 shows the performance of the proposed TSRPWM strategy at high modulation index (mi) of 0.85. It can be shown that the proposed strategy preserves the same output voltage and current of the inverter at both of NORM mode and TSR mode of operation. Therefore, the proposed PWM strategy maintains the inverter to continue its operation with the same output ratings of the inverter and the same output levels as well. Moreover, the voltages of DC-link capacitors remain balanced with slight increase in their ripples. However, the capability of the proposed algorithm to extend the lifetime of the thermally overstressed semiconductor device S_{A11} can be proved by the waveforms of its gating pulses. It is clear that the proposed algorithm has a different switching pattern in the affected device at TSR mode than its switching pattern under NORM mode. This can be interpreted as the proposed algorithm optimizes the power losses through the thermally overstressed switch S_{A11} .

The behavior of the proposed TSRPWM strategy with TSD in S_{A11} at low mi of 0.45 is shown in Fig. 3.10. In the operation with $mi < 0.5$, the inverter operates only in four regions of R1, R3, R4, and R6 and the output voltage in this case is synthesized by only three vectors $+0.5V_{dc}$, $-0.5V_{dc}$, and zero voltage levels. According to the switching states in Table I, utilizing V_{dc1} in positive half cycle of output voltage, utilizing V_{dc2} in negative half cycle,

and utilizing switching sequences of zero voltage level that do not contain S_{A11} will help to reduce the power losses in the affected device S_{A11} to zero. Therefore, the gating pulses of the affected device S_{A11} are switched off and the switch is totally relieved. In addition, the voltage balance of DC-link capacitors is naturally performed as the two sources are equally utilized. It can be seen from Fig. 23.10 that the proposed algorithm preserves the same ratings of V_{out} and I_{out} . Moreover, voltages of DC-link capacitors V_{dc1} and V_{dc2} are kept balanced with slight increase in their ripples.

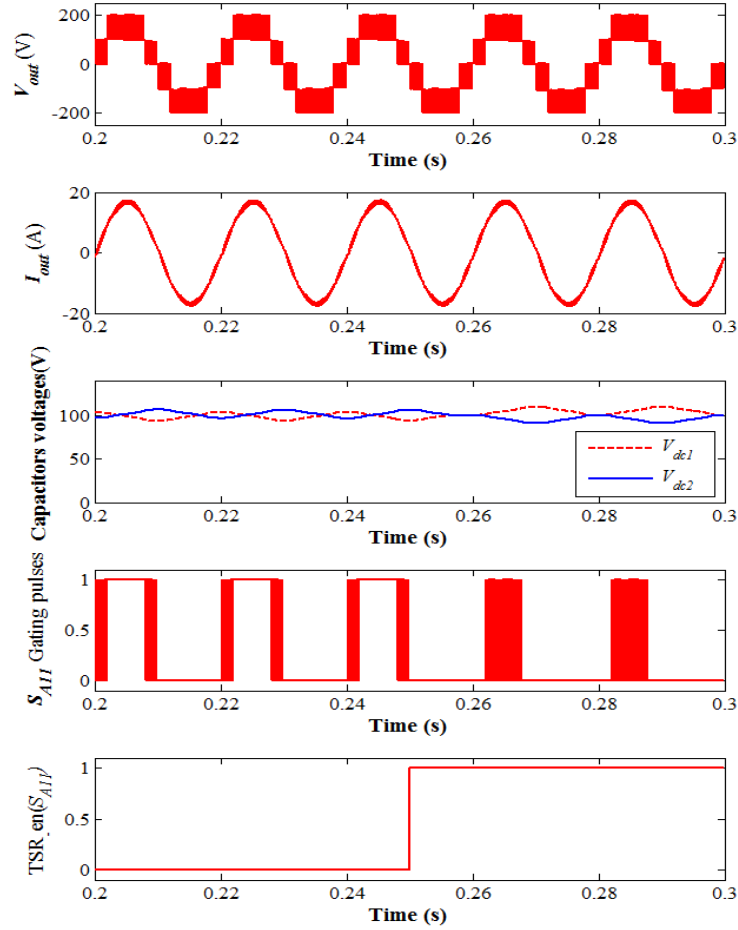


Fig. 3.9. Simulation results of the proposed strategy at TSD in S_{A11} at $m_i=0.85$.

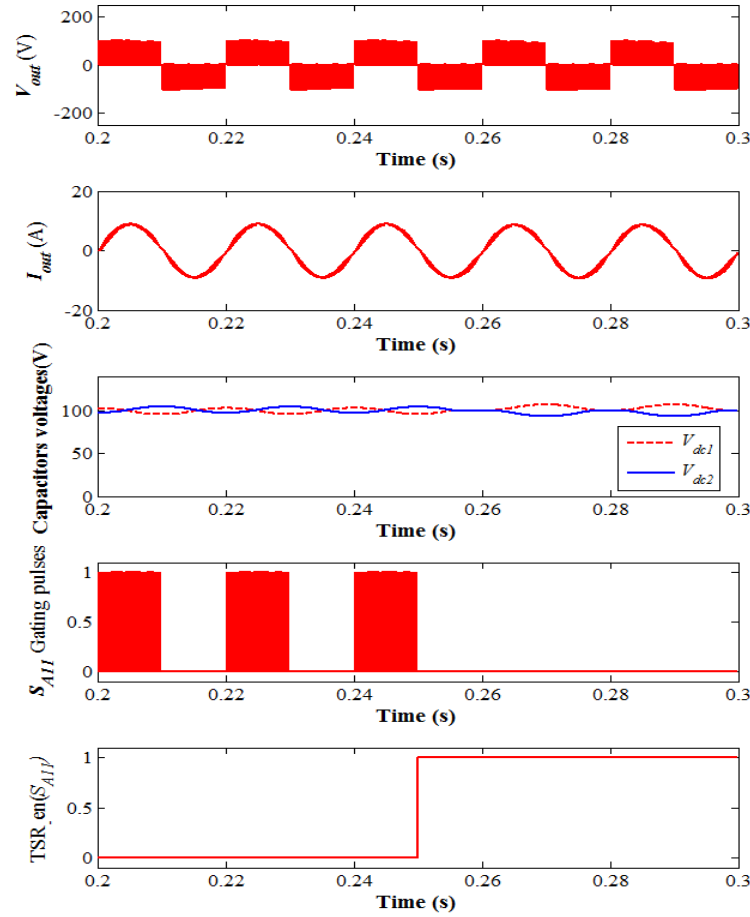

 Fig. 3.10. Simulation results of the proposed strategy at TSD in S_{A11} at $mi=0.45$.

Table 3-2

Parameters for simulation and experimental study.

DC-link voltage V_{dc}	200 V
DC-link capacitance C_1, C_2	2500 μ F
Output frequency f_i	50 Hz
Switching frequency f_s	5 kHz
Output load R, L	10 Ω , 3 mH
Heatsink temperature T_h	60°C
Total thermal resistance between junction and case $\Sigma R_{th(i)}$	2.78°C/Watt
Thermal resistance between case and heatsink $R_{th(c-h)}$	1.4°C/Watt

The lifetime of power semiconductor devices is mainly affected by their junction temperature, and temperature fluctuation [14]. A comparison of the power losses through the thermally stressed device under both of NORM mode and TSR mode at different modulation indices is shown in Fig. 3.11. It can be seen that a significant reduction of the power losses through the affected device S_{A11} can be obtained by the proposed TSRPWM strategy at whole modulation indices range. Thereby, relief of thermal stresses of the affected device is obtained, while maintaining full-rated operation of the inverter. Fig. 3.12(a) shows the junction temperatures of the affected devices under normal mode and overstressed mode at different modulation indices using the thermal parameters in Table 3.2. As a direct benefit of reducing the power losses through the affected device S_{A11} , the proposed TSRPWM method provides a lower T_j and ΔT_j for full mi range. As a result, the corresponding lifetime of stressed device in multilevel inverters has been extended, which verifies the feasibility of the proposed strategy.

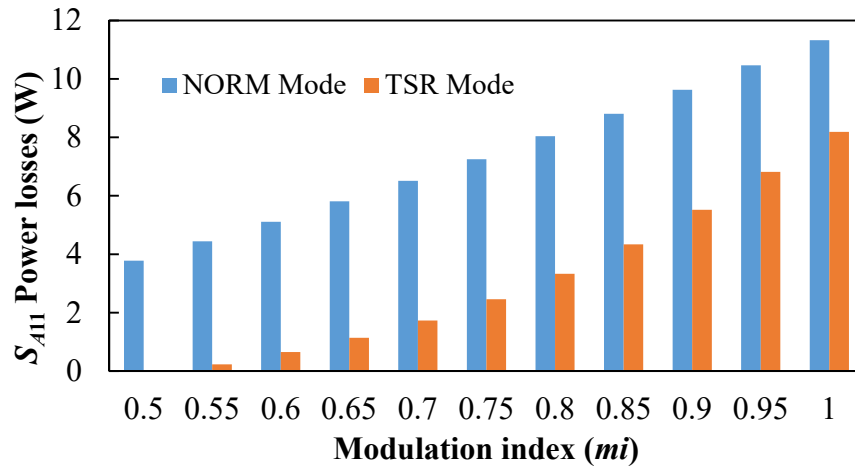
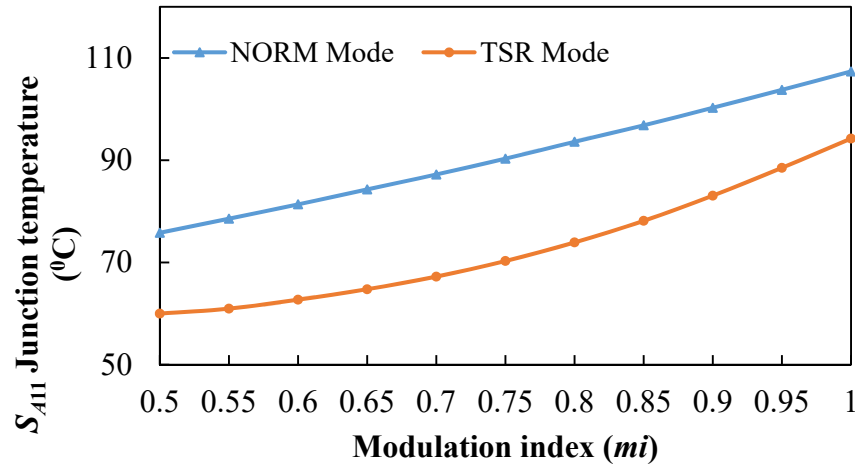
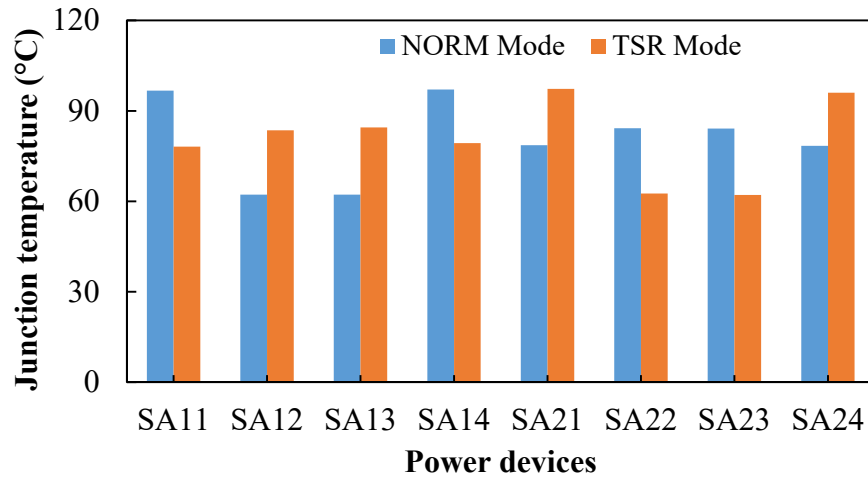


Fig. 3.11. Comparison of power losses in S_{A11} under NORM mode and TSR mode at different mi .

An effective reduction of the thermal stresses of the affected IGBT switch S_{A11} has been fulfilled and the power losses are redistributed and relocated to other less stressed and healthy switches as a result. The estimated junction temperature of all the power switches in the inverter are shown in Fig. 3.12(b) at mi of 0.85. The relocation of power losses is required in TSR mode to preserve the same operation of the inverter without a compromise of its output power ratings and its number of the output levels and without adding extra devices or complex controls.



(a)



(b)

Fig. 3.12. Estimated junction temperature under NORM mode and TSR mode of: (a) S_{A11} at different mi , and (b) Power devices at $mi=0.85$.

In the second case study, it is assumed that there are a TSD in IGBT S_{A12} in leg A1 of the inverter ($\text{TSR_en}(S_{A12})=1$) at time 0.25 seconds. Fig. 3.13 shows the performance of the proposed TSRPWM strategy at high mi of 0.85. According to Table 3.1, the output voltage can be generated by using the source V_{dc1} in the positive half cycle, whereas V_{dc2} is utilized in the negative half cycle. Therefore, no gating signals are required for the switch S_{A12} , and the switch is effectively relieved.

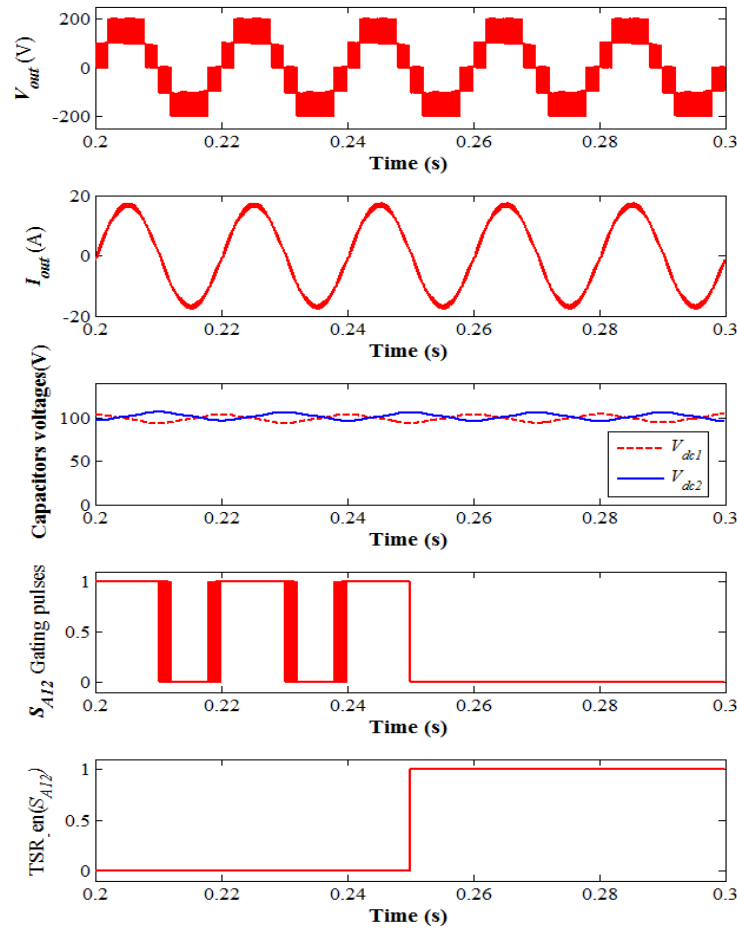


Fig. 3.13. Simulation results of the proposed TSRPWM strategy at TSD in S_{A12} and $mi=0.85$.

It is clear from Fig. 3.13 that the proposed TSRPWM strategy preserves the same V_{out} , the same I_{out} of the inverter, and the same number of output levels. The voltage balance of DC-link capacitors is performed naturally as the two sources V_{dc1} , and V_{dc2} are equally utilized during the line period. Moreover, the gating pulses of the device are shown to ensure the effectiveness of the proposed method.

3.7 Experimental Results

The feasibility evaluation of the proposed TSRPWM strategy is performed experimentally. The parameters of the selected case study are the same of simulation studies, which are listed in Table II. The experimental setup of the inverter and the controller are shown in Fig. 3.14. The proposed control algorithm is implemented using a floating point digital signal processing unit (TMS320F28335). The voltages and currents are measured using LV 25-P, and LEM LA 50-P transducers, respectively. A digital signal is fed to the controller to emulate the flag of increased thermal stresses $TSR_en(S_{Axy})$ in power semiconductor devices.

Fig. 3.15 shows the experimental results of the proposed TSRPWM at TSD in S_{A11} and high modulation index ($mi=0.85$). It is evident that the output voltage V_{out} , the output current I_{out} , and the power rating of the inverter remains the same without derating operation. Thermal stresses relief can be observed from the difference in the switching signals of the affected device S_{A11} . Based on the redundancy among switching states of the multilevel inverter, the proposed strategy operates the inverter with the switching sequence that have minimum power losses through the affected device. Therefore, there are no application limitations of the proposed strategy and it is suitable for several applications

with high reliability demands.

In addition, the proposed TSRPWM has maintained voltage balance over DC-link capacitors. However, it can be observed that TSR mode has a little increase in the ripples of DC-link capacitors' voltages compared to NORM mode. This is because that the main objective of the control algorithm in NORM mode is to achieve voltage balance of DC-link capacitors. Whereas the operation of the proposed algorithm in TSR mode is divided to two regions; (1) In the regions that utilize the stressed device, the proposed algorithm selects the optimum switching sequence for achieving TSR; (2) In the other regions that do not utilize the affected device, the proposed strategy selects the optimum switching sequence for voltage balance of DC-link capacitors. Therefore, voltage balance of DC-link capacitors is achieved in part of the line period in TSR mode, whereas it is performed in whole of the line period in NORM mode.

Moreover, the proposed strategy is tested with TSD in S_{A11} at low modulation index ($mi=0.45$) and the results are shown in Fig. 3.16. The output current and voltage remain the same without reduction in both NORM mode and TSR mode. Besides, voltage balance of DC-link capacitors is preserved in both modes. However, it can be seen that there are no gating signals are fed to the device after TSD in the device. This emphasis that the affected device is totally relieved at low mi range as there are a full redundancy of the switching states that utilizes S_{A11} device. The experimental results assure the feasibility of the proposed strategy at whole mi range.

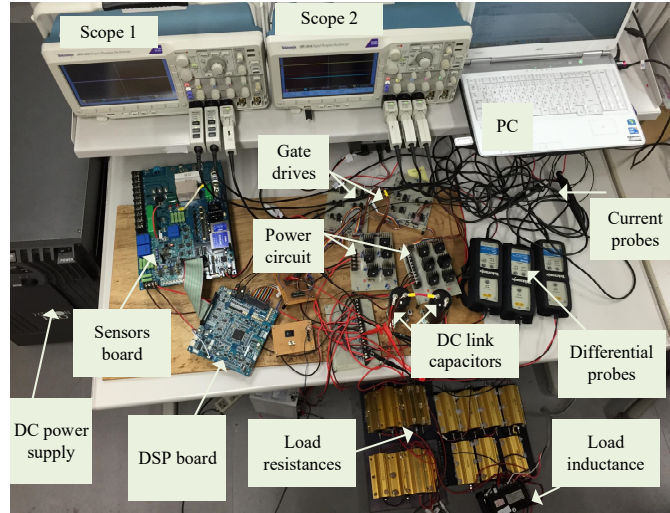
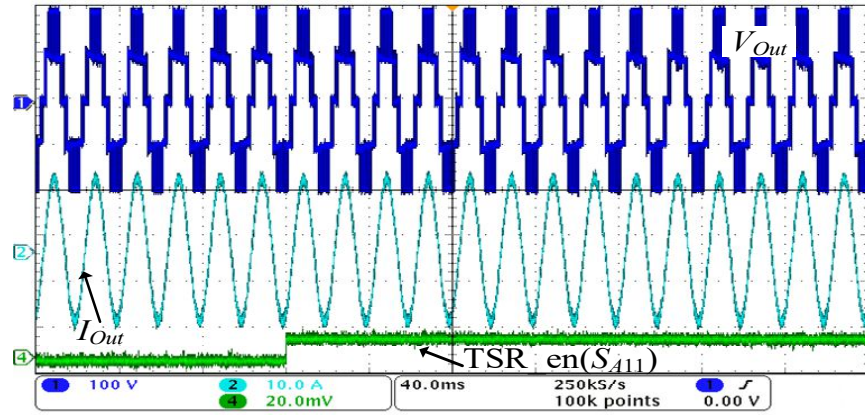
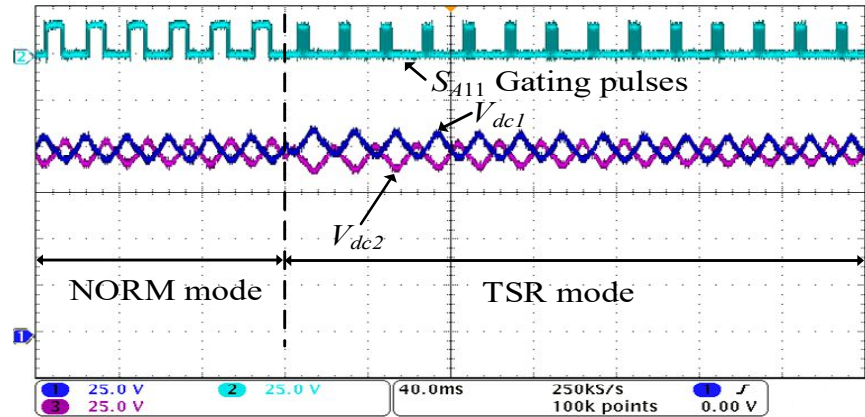


Fig. 3.14. Experimental setup of the inverter and the controller.



(a)



(b)

Fig. 3.15. Experimental results of the proposed strategy at TSD in S_{A11} and $m_i=0.85$: a) V_{out} , I_{out} , and $TSR_{en}(S_{A11})$, and b) V_{dc1} , V_{dc2} , and S_{A11} gating signals.

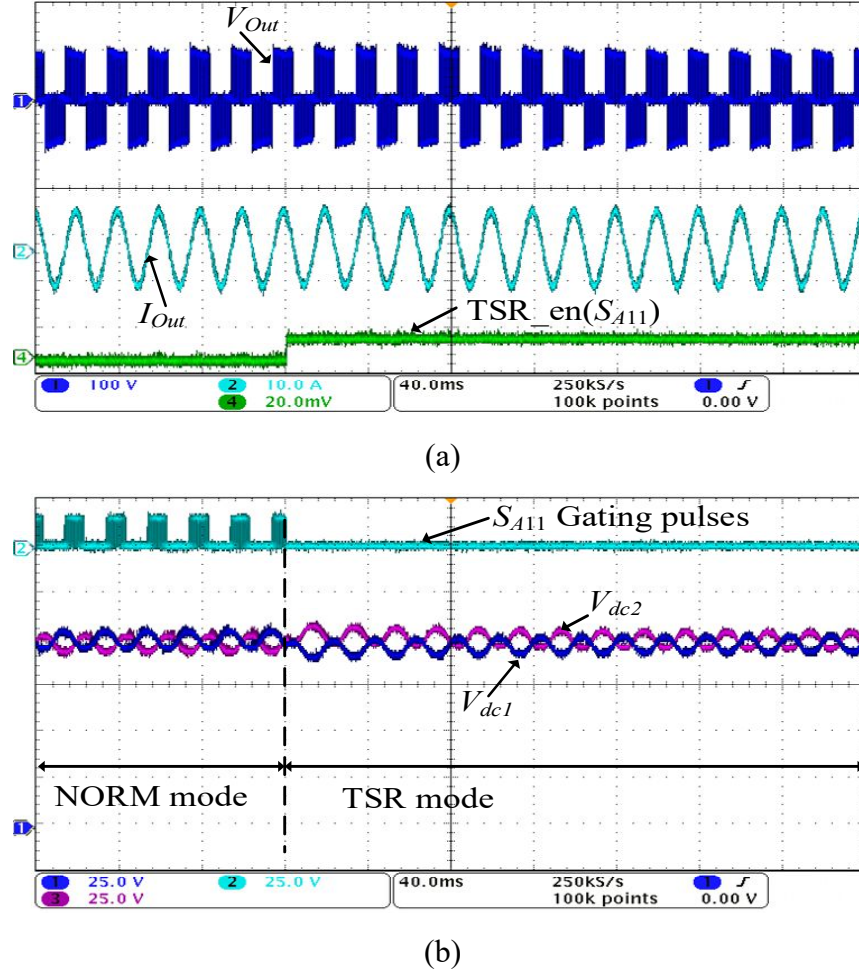


Fig. 3.16. Experimental results of the proposed strategy at TSD in S_{A11} and $m_i=0.45$: a) V_{out} , I_{out} , and $TSR_en(S_{A11})$, and b) V_{dc1} , V_{dc2} , and S_{A11} gating signals.

The thermal behavior of proposed strategy is tested experimentally using IR camera. Fig. 3.17 shows the recorded junction temperature of S_{A11} under NORM mode and TSR modes at $m_i=0.85$. It is clear that TSR mode has lower junction temperature than NORM mode. Relief operation is performed for the stressed device S_{A11} using the proposed TSRPWM and the steady state T_j difference between the two modes is about 10°C . Hence, operating lifetime and long term reliability of the multilevel inverter are robustly improved with T_j reduction using the proposed algorithm. Fig. 3.18 shows comparison of the THD in the output currents in NORM mode and TSR mode with TSD in S_{A11} and $m_i=0.85$. A relatively

slight increase in the THD with TSR mode. The NORM mode has THD in the output current of 5.32%, while TSR mode contains THD of 5.49%.

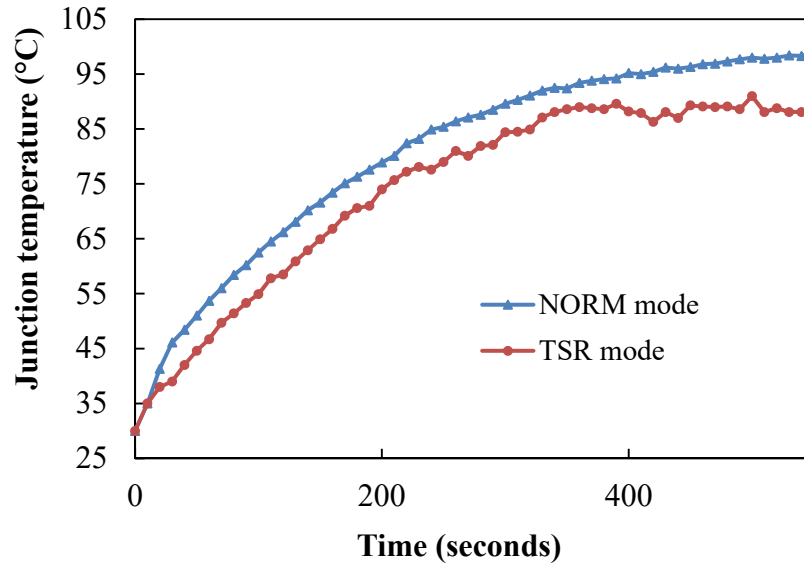


Fig. 3.17. Experimental junction temperature results at TSD in S_{A11} and $m_i=0.85$.

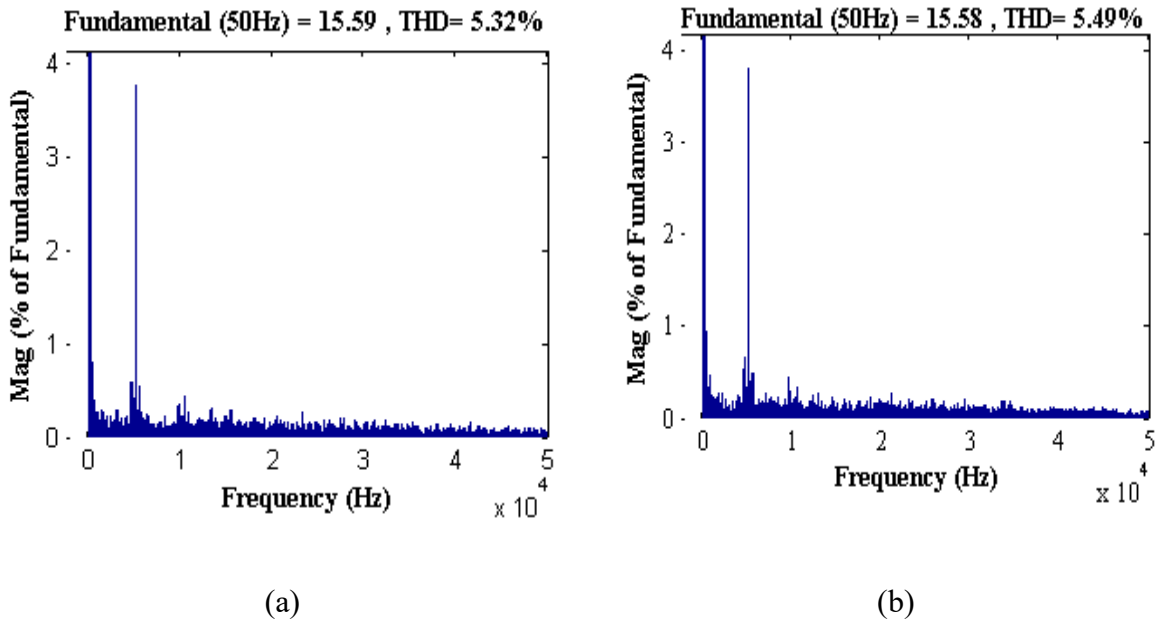
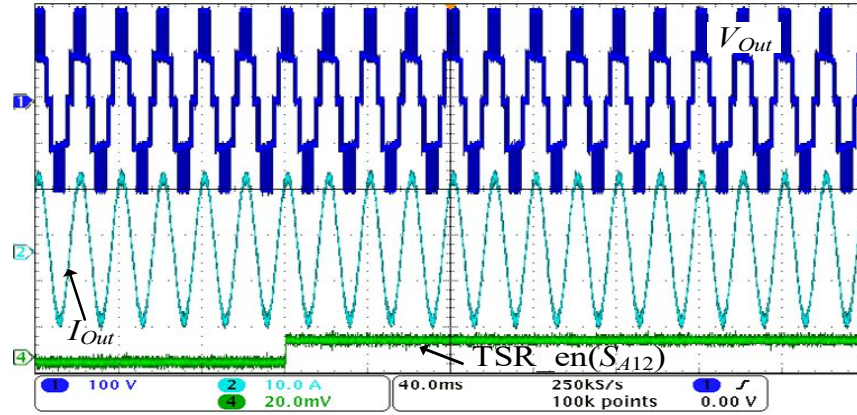
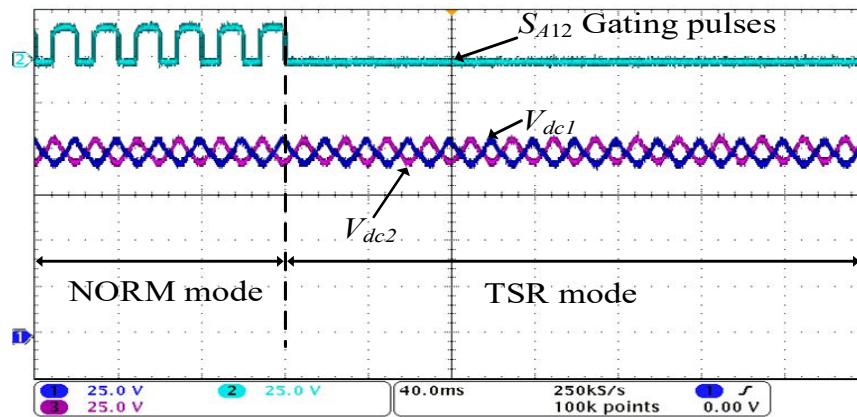


Fig. 3.18. THD comparison of the proposed algorithm at: (a) NORM Mode, and (b) TSR Mode.

Additional test case study is performed experimentally with TSD in S_{A12} at $mi=0.85$ and the results are shown in Fig. 3.19. Preservations of the output ratings including V_{out} , I_{out} , and voltage balance over DC-link capacitors are guaranteed using the proposed strategy. Regarding TSR, the affected device is totally relieved at whole modulation indices range without interruptions of the output performance. The proposed algorithm is suitable for TSR of IGBT devices at different locations in the inverter. Furthermore, the proposed strategy can be generalized for different multilevel inverters structures.



(a)



(b)

Fig. 3.19. Experimental results of the proposed strategy at TSD in S_{A12} and $mi=0.85$: a) V_{out} , I_{out} , and $TSR_en(S_{A11})$, and b) V_{dc1} , V_{dc2} , and S_{A11} gating signals.

3.8 Comparison of TSR Strategies

Based on the literature review given in Section 3.2 and the performance of the proposed algorithm, Fig. 3.20 proposes a criterion for evaluating and comparing the performance of different thermal stresses relief methodologies. The overall performance of each methodology is represented by radar view diagram. This radar diagram contains five vertex properties such as complexity, rating, cost, THD, and TSR. Due to the lack of precise evaluation for each criterion, relative comparisons between various TSR methodologies with respect to each other have been carried out. Each vertex property grades the performance of the tested topology from four levels. In this diagram, favorable vertex property of the methodology is located near the periphery of the radar diagram, while unfavorable vertex property is directed towards the origin of the diagram. The main factors for quantifying different performance criteria are shown in Table 3.3. A discussion of each vertex property is provided as follows:

- a) Complexity: The complexity criteria is a measure of the difficulty in implementing the TSR strategy. It represents a key factor in comparing various approaches of the literature with the proposed TSRPWM method. The quantification process of complexity is performed according to the number of complex computations and controls in each strategy. Each added complexity reduces the score of the strategy. For example, in [56], a simple PI controller is needed to adjust the current reference for achieving TSR. However, driving the added cooling device that requires a precise thermal modelling of the cooling system adds complexity to the strategy in [57]. In [47], the adjustment of the percentage share for the interleaved converters requires precise measurements of the on state resistance of IGBTs in all the interleaved

converters. Moreover, different power sharing between the interleaved converters results in circulating currents that require additional control and filters as investigated in [70]. However, in [62], the complexity occurs when adjusting and estimating the injected common mode voltage to relieve different IGBTs locations. In SVPWM based method in [65], voltage balance of DC-link capacitors under TSR modes requires complex calculations to replace the space vectors. Based on the evaluation of implementation complexity of SVPWM methods in [71], [72], SVPWM methods exhibit two additional complexities in defining the region of reference vector in the space vector diagram and in calculating the switching times of the space vectors. From another side, one of the main advantages of the proposed strategy is that it is based on PWM implementation, which does not have the problems of defining the switching times and operating region [71], [72].

- b) Rating: The rating criteria represents the ability of the TSR approach to preserve the operation of the inverter with the same output ratings under NORM mode and TSR mode. It is highly required to operate the inverters at MPP in renewable energy applications. Rating criteria of various strategies are quantified according to the required level of reducing the output rating. TSR strategies are classified into four levels that represent the same rating, little, moderate, or high reduction of output rating level. In [56], derating of the output power is needed to achieve TSR of the affected devices, and results showed that about 50A reduction of the output current is required to achieve 50% reduction of the power losses in the device. However, in [57] and [47], there are no changes in the output ratings before and after TSD because thermal relief is achieved based on adding cooling devices, and interleaving of

converters, respectively. Moreover, TSR methods in [62], [65], and the proposed TSRPWM strategy are based on switching states redundancy in multilevel inverters, and no changes in the output ratings are required as a result.

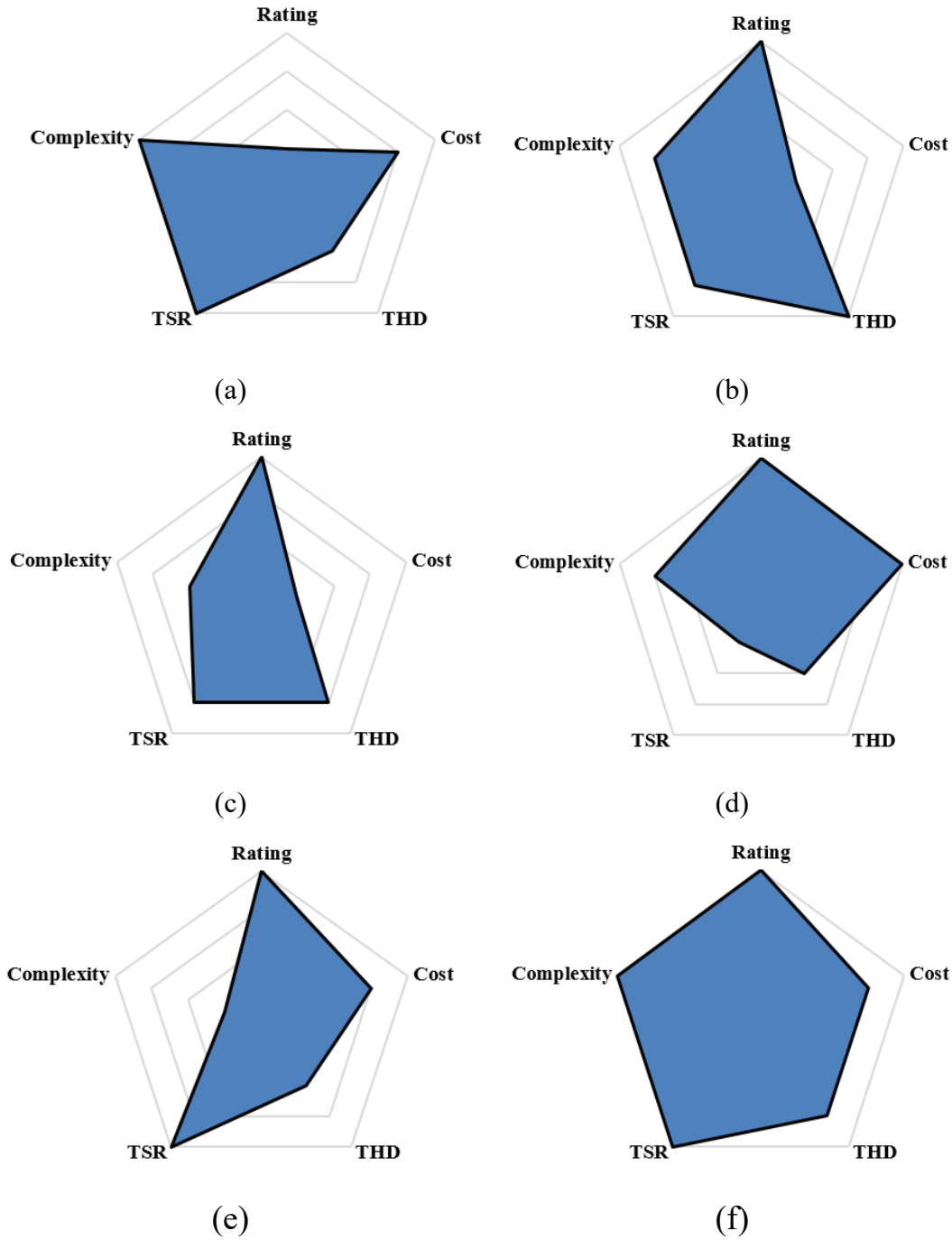


Fig. 3.20. Comparison of TSR strategies. (a) Ref [56]. (b) Ref [57]. (c) Ref [47]. (d) Ref [62]. (e) Ref [65], and Ref [66]. (f) The proposed TSRPWM method

- c) Cost: The cost criteria includes the extra charges for the required additional devices, measurement circuits, component ratings, and powering circuits. Each added device is used to quantify and compare different strategies. Excluding DPWM method, all other approaches requires TSEP estimation circuits. Additionally, in [57], additional costs are required for the added cooling device in addition to its powering and driving circuit. The strategy in [62] has the highest cost and requirements among different TSR methodologies. The cost includes using TSEP circuit, full rating converters for all the interleaved modules, and circulating current filters.
- d) THD: THD measurements are crucial especially in grid connected systems. A relative comparison of the changes in THD value between NORM mode and TSR mode for TSR strategies is carried out because of the different output ratings, output filters, and operating conditions in each strategy. In the analysis, THD changes between NORM mode and TSR mode are represented by four levels that represent the same THD, little, moderate, or high increase in THD, respectively. In [56], a high reduction of the output ratings is required to achieve TSR, however, low output power operation of the inverter increase the THD in the output as investigated in [64]. The same THD is maintained in [57] as there are no change in the output ratings or the modulation technique. However, in [47], the circulating currents in TSR mode add low and high frequency components that make a little increase in the THD in interleaved converters as shown in [73]. Meanwhile, the strategy in [62] is based on DPWM technique that increases the THD in the outputs [74]. In [65], THD has increased in the outputs in order to achieve voltage balance of DC link capacitors and similarly in [66], THD has increased in TSR mode from 3.4% to 7.3%. The proposed

TSRPWM strategy has maintained a little increase in THD from 5.32% to 5.49% that has been verified by simulation and experimental results.

- e) TSR: TSR criteria is the measure of the effectiveness of the TSR approach to reduce the junction temperature of the thermally stressed device. The TSR criteria of strategies is divided to four categories that represent high, moderate, little, or no effective for achieving relief. In [56], results showed that about 50A reduction of the output current can achieve 50% reduction of the power losses in the device, which guarantee a high TSR of the affected device. However, in [57], controlling the added cooling device has effectively maintained the same junction temperature with an output current rise from 6A to 9A. In [47], a decrease in T_j from 49°C to 43°C has been achieved. However, unequal share of the interleaved modules results in circulating currents between modules and additional power losses in switching devices are obtained [70], [73]. Moreover, circulating currents increase at high difference in percentage sharing between modules. From another side, DPWM based methods represents the worst approach for achieving TSR of thermally stressed devices. This is due to that DPWM strategy is concerned with improving the overall inverter switching power losses, regardless of the individual device power losses or the added conduction power losses. Results of SVPWM method in [65] have showed an effective TSR of about 10°C reduction in T_j of the affected device. The feasibility of the proposed TSRPWM to achieve TSR of switching devices has been confirmed with simulation and experimental measurements. A reduction of more than 12°C has been achieved for the whole operating mi range of the inverter.

Fig. 3.20 illustrates the graphical implementation of the radar diagram shape for the addressed methodologies compared to the proposed TSRPWM strategy. It is clear the proposed algorithm achieves the full power rating during NORM and TSR modes, low system complexity, high effective TSR, and little increase in THD and cost compared to the addressed ones. Therefore, the proposed methodology presents its efficacy and effectiveness for motor drives and grid connected systems.

Table 3-3

Parameters for quantifying different performance criteria for TSR strategies.

Criteria	Quantification basis	Score reduction
Complexity	No extra complexity	0
	Control (controlling added device or DC-link capacitors' voltages)	1
	Adjusting TSR controller (percentage share or added CMV voltage)	1
	Complicated arithmetic operations	1
Cost	T_j measurement	1
	Additional devices	1
	Additional driving and powering	1
	Increased ratings of converters	1
Rating	No change	0
	Little reduction	1
	Moderate reduction	2
	High reduction	3
TSR	Highly effective	0
	Moderate effective	1
	Little effective	2
	Not effective	3
THD	No change	0
	Little increase	1
	Moderate increase	2
	Highly increase	3

3.9 Conclusion

This chapter has proposed a new carrier-based modulation strategy, called TSRPWM, for single phase multilevel inverters. It retains the same benefits as the conventional carrier PWM methods, i.e., a simple and easy implementation, but presents a significantly reduced power losses and thermal stresses of the stressed semiconductor devices. The main idea of the new proposed strategy is adaptively selecting the redundant switching states in each switching cycle, in order to optimize power losses through the thermally-stressed device. Therefore, both of the junction temperature and temperature cycling of the stressed device are reduced by the proposed strategy compared with normal mode operation of the device. The results of simulation and experimental prototypes are conformed and verified the new proposed concept. A generalized implementation of the proposed TSRPWM, to provide thermal stresses relief for any of the components and for any n-level inverters, is also presented. Moreover, the proposed strategy maintains the inverter operation with the same output ratings, and voltage balance over DC-link capacitors. Finally, the performance of the proposed strategy is compared with the prominent strategies in literature, and the distinction of the proposed strategy has become clear.

Chapter 4

Developing New Lifetime Prolongation SVM

Algorithm for Multilevel Inverters with

Thermally-Aged Power Devices

4.1 Overview

Research concerns have grown towards precede diagnosis and prognosis of faults in power converters that result from thermal overheating problems of semiconductor devices. These problems directly affect the overall system availability and reliability as well. Many research work in the literature have addressed these problems. However, almost all of them suffer from major challenges such as increased components count, reduced output current ratings, reduced output voltage levels, and unbalanced voltages over the DC-link capacitors. These challenges impede the maximum energy harvesting, especially in renewable energy systems. In this chapter, a novel space vector modulation (SVM) algorithm has been proposed for lifetime prolongation of thermally-aged power semiconductor devices in multilevel inverters. The proposed SVM algorithm functions to alleviate the affected device. The feasibility of the proposed method has been verified by simulation and experimental results on the three-phase three-level T-type inverter and compared to the previously addressed approaches. The proposed algorithm maintains the same components count, the same output ratings, the same output levels, and balanced capacitors' voltages as well.

4.2 Introduction

Recently, analysis of fault prognostic in power converters has been widely investigated in many reports. In these reports, the reliability of power semiconductor devices has been recognized as the most serious challenge in evaluating the reliability of the overall system. Industry-based reliability surveys have reported that power electronics components are the most vulnerable parts of power converter systems [7]. About 55% of power semiconductor devices failures are caused by thermal stresses, including junction temperature and temperature fluctuations [4]. These failures are due to the existence of different thermal expansion coefficients of layers' materials that form the semiconductor device. Therefore, continuous overloading and power cycling on these layers result in cracks, voids, and delamination of power devices' components [75], [76]. As a result, the thermal resistances of insulated-gate bipolar transistor (IGBT) devices increase, and correspondingly their junction temperature. It is stated that power cycling increases the equivalent thermal impedance of IGBT devices by more than 20% above its normal values [15].

Therefore, increased potentials have been devoted to developing more reliable power electronics systems with prolonged lifetime regardless of faults and thermal aging conditions. Comprehensive surveys on fault tolerant operation of power electronics converters were provided in [77]. Most of the addressed solutions included redundant switches, legs, and/or modules [78]–[80]. These solutions are expensive, and complex. In addition, they increase the converter footprint and component counts. Alternative approaches for fault tolerant control of parallel or interleaved converters were developed by controlling the percent of power sharing between converters [47], [81]. The existence of different current paths makes possible to keep converter action without degrading

operation or including redundant components. In addition, full-scale converters are needed to avoid overloading in faulty conditions. Moreover, parallel operation of converters is being avoided due to the existence of circulating currents problem and extra control complexity.

On the other hand, some other methods for precede fault tolerant control were developed to extend converter lifetime by managing the thermal behavior of thermally-aged IGBT devices through controlling their power losses [56], [57], [82]. In these techniques, the operating junction temperature of IGBT has been sensed and controlled to be less than the maximum junction temperature provided by IGBT manufacturers. In [57], thermoelectric cooling (TEC) device has been added between thermal grease and heatsink of IGBT device to manage and to cool its junction temperature. Nonetheless, adding TEC devices increases the total cost, volume, and power consumption of the system. However, the active thermal management method in [56] has limited the operational junction temperature of inverter components in motor drive applications by reducing the output currents of the inverter. This method degrades power operation and thereby it is not appropriate for full power conditioning applications.

Basically, redundancy property in multilevel inverters (MLIs) represents another vital solution for fault tolerant operation. Multilevel inverters can continue their operation using redundant vectors. A fault tolerant methodology based on SVM for post-fault compensation was introduced in [82] for three-level inverters, wherein the faulty leg was attached to the neutral point (NP) and the number of levels of the line voltages was reduced. Furthermore, reducing the number of the output levels requires complex calculations. On another side, SVM was utilized for reducing thermal stresses on IGBT devices through

controlling their power losses such as discontinuous space vector modulation (DSVM) [83], [64]. DSVM can improve the efficiency of the whole inverter by reducing the switching power losses. However, DSVM is not effective for relieving a single thermally-aged semiconductor device. SVM schemes for loss redistribution between different semiconductor devices were addressed in [59]. Although these SVM schemes can simultaneously reduce and equalize power losses in semiconductor devices, they cannot effectively relieve a single thermally-aged device. A proper SVM algorithm was introduced in [66] for lifetime expansion of IGBT devices through selecting the current path with the least conduction or the least switching losses of the available switching sequences. However, this algorithm exhibits a single objective function that cannot maintain voltage balance of DC-link capacitor. Moreover, it cannot be generalized and applied to any n -level inverter. Another thermal management SVM algorithm for enhancing the reliability of multilevel inverters was developed in [65]. However, additional voltage stresses on semiconductor devices and DC link capacitors were introduced in this method to achieve the voltage balance of DC-link capacitors. Moreover, asymmetry of output line voltages increases the total harmonic distortion (THD) and causes biased magnetism problems.

Indeed, among different modulation techniques, SVM draws more concerns: it eliminates the use of triangular carrier waveforms; it gives more flexibility in optimizing switching waveforms through selecting redundant switching states and adjustable duration times; and it is more suitable for digital implementation [84]. A generalized diagram of the SVM-controlled n -level three-phase inverter is shown in Fig. 4.1. For any n -level inverter, the space vector diagram contains $6(n-1)^2$ triangles with total n^3 switching states [84].

Therefore, considerably enhanced performance can be achieved for multilevel inverters, especially with higher numbers of levels and the corresponding increased number of redundant switching states. Several schemes for optimum SVM design have been developed in the literature to improve the performance of multilevel inverters including voltage balance of DC-link capacitors, reduction of common mode voltages (CMV), reduced THD, minimized losses, and fault tolerant control [59], [85].

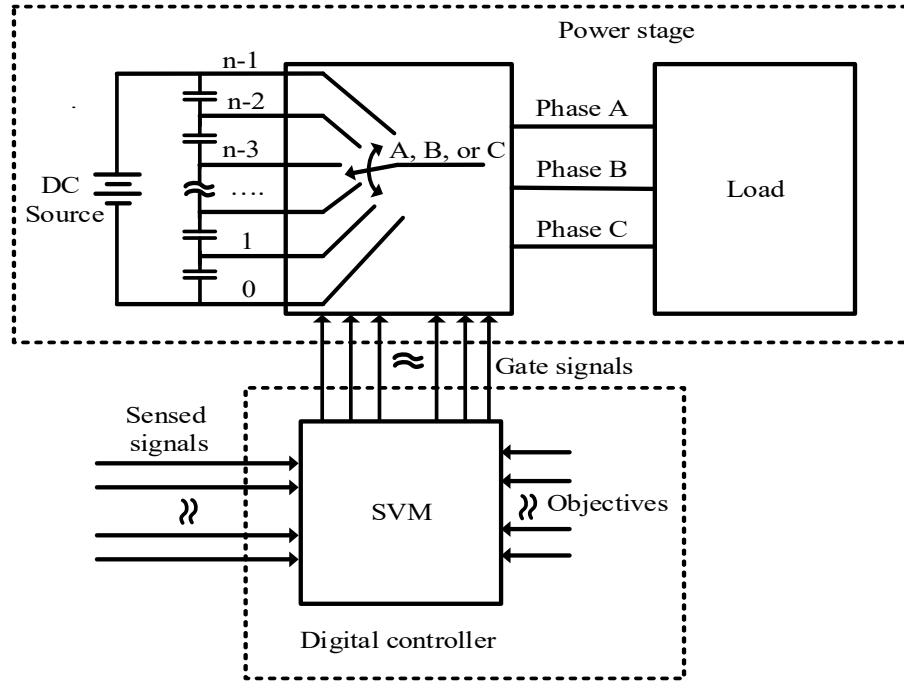


Fig. 4.1. Block diagram of SVM-controlled n -level three-phase inverter.

It is clear from the above discussion that the existing methods for lifetime extension impose degraded performance of multilevel inverters in the form of reduced number of levels, reduced output currents, voltage unbalance of the DC-link capacitors, etc. Therefore, developing generalized fault tolerant methods that have the capability to keep the output voltage levels and capacitors voltages balance are highly essential.

This chapter proposes a new SVM algorithm for lifetime prolongation of thermally-aged semiconductor devices in multilevel inverters. The proposed algorithm can maintain the same number of the output voltage levels, output current and voltages balance of the DC-link capacitors as well. Moreover, the proposed algorithm is generalized to be applied to any power semiconductor devices in n -level inverter with a simple modification in the conventional SVM algorithms. The proposed algorithm is validated using simulation and experimental results for the three-level T-type inverter. In addition, comprehensive comparisons with the existing lifetime extension methods are performed in order to verify the effectiveness of the proposed algorithm.

This chapter is organized as follows: Section 4.3 explains the principles of SVM and lifetime prolongation of power semiconductor devices. Section 4.4 provides the details of the proposed lifetime prolongation SVM methodology and its implementation. The feasibility verifications of the proposed SVM algorithm on three-level inverters are discussed in Section 4.5. Section 4.6 presents the experimental results and comparison with existing methods to validate the proposed SVM algorithm. The conclusions are summarized in Section 4.7.

4.3 Principle of SVM and Lifetime Prolongation for Multilevel Inverters

4.3.1 SVM for n -Level Inverters

Normally, in SVM, the nearest three-vectors (N3V) are utilized to synthesize the reference vector for the n -level inverter. Fig. 4.1 shows a schematic diagram of the SVM-controlled n -level inverter. The reference vector is related to the N3V as follows:

$$V_{ref}T_s = V_1d_1T_s + V_2d_2T_s + V_3d_3T_s \quad (4.1)$$

$$d_1 + d_2 + d_3 = 1 \quad (4.2)$$

where V_1 , V_2 , and V_3 are the N3V to the reference vector V_{ref} ; d_1T_s , d_2T_s , and d_3T_s are their corresponding dwelling times during commanded switching cycle T_s ($=1/f_s$); $d_i=T_i/T_s$ ($i=1, 2, 3$). The inverter output is represented by (4.3) [86]:

$$V_{out} = V_{dc} \cdot (S_a + S_b e^{j\frac{2}{3}\pi} + S_c e^{j\frac{4}{3}\pi}) \quad (4.3)$$

where V_{dc} represents input DC voltage; S_a , S_b , and S_c represent the corresponding switching states for phases A, B, and C, respectively. Whereas S_a , S_b , and S_c can take the value of 0, 1, ..., $n-1$ and their corresponding three-phase output voltages are $S_a \cdot V_{dc}/n-1$, $S_b \cdot V_{dc}/n-1$, and $S_c \cdot V_{dc}/n-1$, with respect to the negative terminal of DC source. All the possible output vectors using (4.3) and their consistent inverter output states can be collected in a single space vector diagram as shown in Fig. 4.2 for three-level inverters.

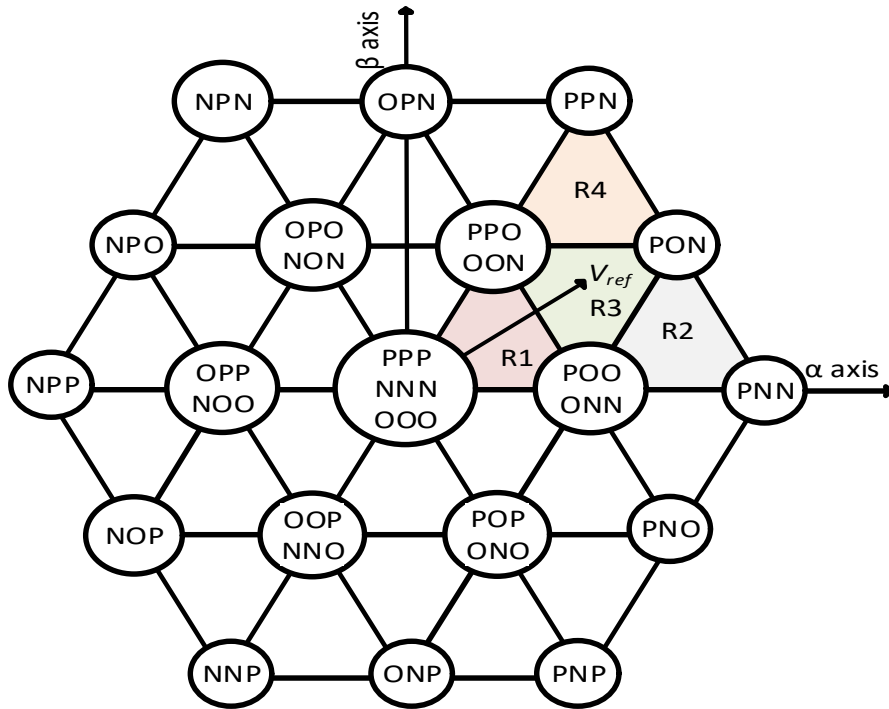


Fig. 4.2. Space vector diagram for the three-level inverters.

Various switching sequences can be constructed using different redundant vectors and hence various switches combinations can be utilized. As a result, dissimilar performances can be obtained from different combinations such as NP voltage, THD, power losses, CMV, etc. Therefore, optimized design and selection of redundant vectors, dwell timing, and switching sequence are highly required to enhance the performance of multilevel inverters.

4.3.2 Lifetime Prolongation of Power Semiconductor Devices

The lifetime expectancy of power semiconductor devices can be expressed as a function of the number of cycles that they can perform effectively. In [14], the authors summarize the main factors that affect the lifetime of power semiconductor devices. These factors are junction temperature T_j , temperature fluctuations ΔT_j , and time duration of the ON-state of the inverter output current. The number of cycles to failure N_f of power semiconductor devices can be calculated as in (4.4) [14]:

$$N_f = A. (\Delta T_j)^\alpha. \exp\left(\frac{E_a}{K_b T_j}\right) \quad (4.4)$$

where α and A are constants that can be obtained from power cycling tests, E_a represents activation energy and K_b represents Boltzmann constant. It is clear from (4) that the lifetime of power semiconductor devices can be prolonged by reducing their thermal stresses, including T_j and ΔT_j . Thermal stresses result from power losses through the device and they are calculated in the manuscript as in [14]. In addition, a more accurate power losses estimations can be obtained using the detailed devices' parameters that are available in manufacturer's datasheets. The analytical estimations of the devices' power losses are given in details in [43]. Then, the power losses are calculated for N available switching sequences in every switching period T_s .

4.4 The Proposed SVM Algorithm

4.4.1 The Proposed SVM Algorithm

Recent real-time junction temperature estimation methods that are based on thermo-sensitive electrical parameters (TSEP) techniques represent cost-effective solutions for detecting the junction temperature of power semiconductor devices [68], [76], [87], [88]. The measured junction temperature is fed to overheating fault detection algorithm, which generates an OHF_Flag signal in case of the overheating condition. In this manuscript, the problem of the overheating condition detection has not been tackled; it is assumed that reliable T_j information is available. Moreover, it is simulated and implemented by an external ON/OFF switch.

The thermal behavior of power semiconductor devices is a direct function of their power losses [14]. If thermal overheating is detected in one of the semiconductor devices, the proposed algorithm is applied to relieve the device and to prolong its lifetime consequently. The proposed lifetime prolongation algorithm depends on utilizing the redundancy property between different switching states of the multilevel inverter and the flexibility provided by SVM. The redundant space vectors of the n -level inverter can produce the same line voltages, however, they have different current paths and connections of semiconductor devices. Therefore, they can be optimized to obtain particular system performances such as NP voltage control of the inverter and particular semiconductor stresses such as power losses through the devices.

The proposed algorithm continuously evaluates and minimizes a cost function Λ of the power losses in the thermally-aged device, which helps to identify the optimal switching sequence for protecting and relieving the device. At the beginning of each switching cycle

T_s , the reference vector is read and the dwelling times are calculated for the N3V using (4.1) and (4.2). If an overheating is detected in one of the semiconductor devices, the OHF_Flag is set to 1 and the proposed algorithm is enabled. In every switching period T_s there are N -valid switching sequences set $S = \{S_1, S_2, \dots, S_N\}$ in the current location of the reference vector. Their corresponding power losses set $P_{loss,device} = \{P_{loss,device}(S_1), P_{loss,device}(S_2), \dots, P_{loss,device}(S_N)\}$ through the thermally-aged device are calculated for each switching sequence in S . The calculations of $P_{loss,device}$ set can be implemented in parallel. Thus, the entirely required time to execute the algorithm can be reduced. Finally, the proposed algorithm selects the sequence that has minimum Λ . The cost function can be implemented as in (4.5):

$$\min \Lambda(S) = P_{loss,device} * (Z_{th(j-c)} + Z_{th(c-a)}) + T_a \quad (4.5)$$

where $Z_{th(j-c)}$ and $Z_{th(c-a)}$ represent the Thevenin equivalent thermal impedances between junction and case, and between case and ambient, respectively. T_a denotes to the operating ambient temperature. Hence, to relieve the affected switch, the cost function in (4.5) is required to be continuously minimized every switching period. A schematic diagram of the proposed lifetime prolongation SVM algorithm for the n -level inverter is shown in Fig. 4.3. The inverter is controlled by normal SVM algorithm until the detection of thermal overheating condition (OHF_Flag=1). The sensed signals of the inverter are used with the sequence set S to estimate the corresponding power losses set $P_{loss,device}$ in the affected switch. Then the optimizer selects the switching sequence with the minimum power losses in the affected device. Finally, the selected S_{opt} is transferred to gate signals to drive the IGBT switches of the inverter.

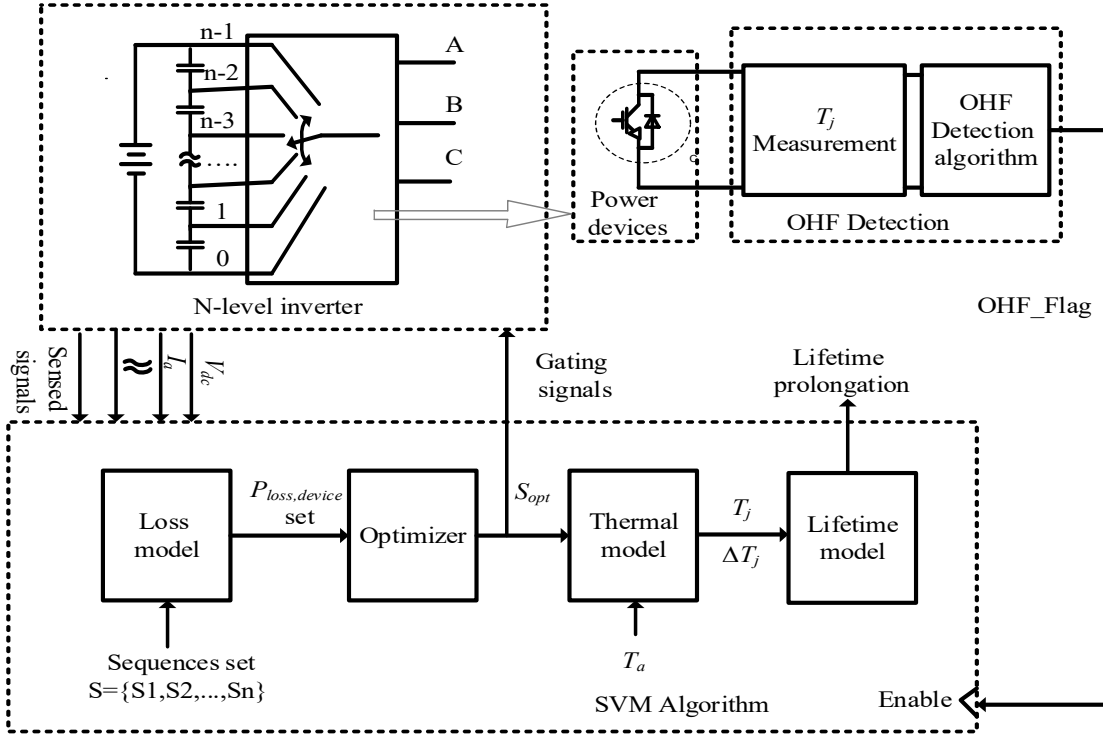


Fig. 4.3. A schematic of the proposed SVM algorithm for lifetime prolongation of power semiconductor devices in n -level inverter.

4.4.2 Preserving Voltage Balance of DC-Link Capacitors

Normally, the DC link capacitors are controlled in order to maintain their voltages at equal levels of $V_{dc}/n-1$. Various voltage vectors can be classified according to their effects on the voltages of DC-link capacitors to 1) Charging voltage vectors, 2) Discharging voltage vectors, and 3) No effect voltage vectors. Although the proposed algorithm selects the optimal switching sequence that relieves the overheated device regardless of voltage balance of DC-link capacitors. In order to preserve voltage balance for DC-link capacitors, the space vector diagram is divided into two regions according to the utilization of the thermally-aged IGBT device. In the sextants that utilize the thermally-aged device, the proposed algorithm selects the optimum switching sequence to prolong the lifetime of the thermally-aged device as in the previous section. However, in the other sextants that do not

utilize the thermally-aged device, the proposed algorithm selects the switching sequence and durations of redundant vectors according to voltages differences of the DC-link capacitors. Therefore, the selected voltage vectors charge or discharge DC-link capacitors according to switching sequences in order to keep the voltages of DC-link capacitors within predefined limit without being increased or decreased.

4.5 Feasibility Verification of the Proposed Algorithm:

For better clarification, the proposed algorithm has been verified on the three-phase three-level T-type inverter system as a case study. Simulation and experimental prototypes have been implemented and compared with the previously addressed approaches.

4.5.1 Applying the Proposed Methodology

Fig. 4.4 shows a representative phase of the three-level T-type inverter. Each phase leg x ($x=a, b, \text{ or } c$) is composed of four IGBT switches ($S_{x1}, S_{x2}, S_{x3}, S_{x4}$). Different switches combinations can be utilized to produce one of three states: [P], [O], or [N] in each phase. Table 4.1 illustrates the switching combinations for obtaining the three states of the inverter. The space vector diagram that is shown in Fig. 4.2 is used to control the three-level inverter outputs. The divisions (R1-R4) in space vector diagram of the three-level inverter are clarified in Fig. 4.2 for the first sextant as an example.

In normal SVM, the dwelling times are equally divided between redundant vectors. Taking region R4 in the first sextant as an example, the resulting switching sequence is shown in Fig. 4.5(a). By assuming that an overheating has been detected in switch S_{a1} in phase A, which is colored in red in Fig. 4.4, and the proposed algorithm is activated. In the current location of V_{ref} (region R4), there are three available switching sequences: 1) S_1 that uses

both redundant vectors ($S_1=\text{OON-PON-PPN-PPO-PPN-PON-OON}$), 2) S_2 that uses only OON redundant vector ($S_2=\text{OON-PON-PPN-PON-OON}$), and 3) S_3 that uses only PPO redundant vector ($S_3=\text{PON-PPN-PPO-PPN-PON}$). The resulting switching sequence set is $S = \{S_1, S_2, S_3\}$. Fig. 4.5(a)-(c) show the switching sequences S_1 - S_3 , respectively. It is clear that the switching sequence S_2 has less conduction power losses than S_1 . Whereas the switching sequence S_3 does not include switching power losses. Then, the power losses set $P = \{P_{loss,sa1}(S_1), P_{loss,sa1}(S_2), P_{loss,sa1}(S_3)\}$ through the thermally-aged switch S_{a1} is calculated and fed to the optimizer, which selects the switching sequence with minimum power losses through S_{a1} . As a result, the proposed algorithm continuously pulls the junction temperature to be less than the maximum operating junction temperature of the IGBT device. The thermal overheating is gradually removed without derating of the inverter and without reducing the number of levels as well.

Furthermore, this strategy employs the redundant voltage vectors for relieving the overheated switch, regardless of their effects on the voltage balance of DC-link capacitors. In regions that do not include switching state P in phase leg A, such as regions of the third and fourth sextants, the redundant vectors and their duration times are adopted to balance the voltages of DC-link capacitors. The duration times of the voltage vectors that discharge C_1 are increased when $V_{dc1} > V_{dc2}$, while the duration times of the voltage vectors that discharge C_2 are increased when $V_{dc2} > V_{dc1}$. Therefore, the voltage balance of DC-link capacitors is preserved without affecting the thermal stresses of the thermally-aged IGBT switch. In addition, ΔV_{cap} remains within the limit and hence the extra stresses on DC-link capacitors and power semiconductor devices are avoided. The same strategy can be applied to other regions and also to overheating conditions of the other power switching devices.

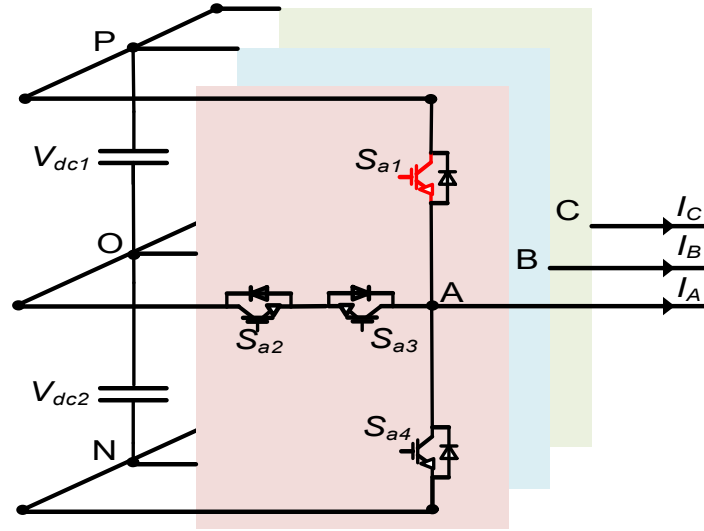


Fig. 4.4. A representative phase of the three-level T-type inverter.

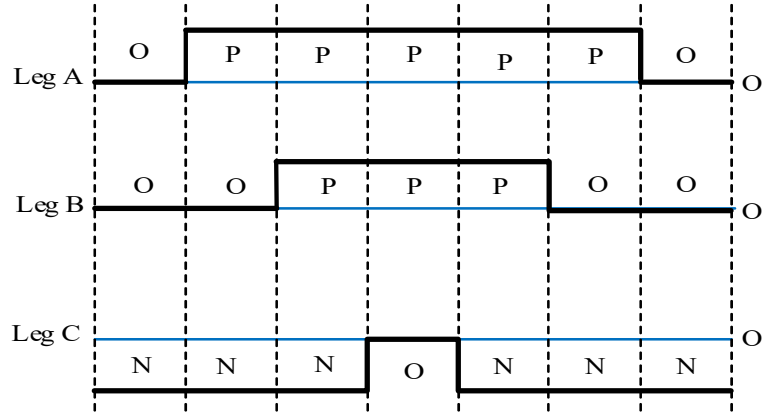
Table 4-1

Switch combinations for different switching states in three-level T-type inverters

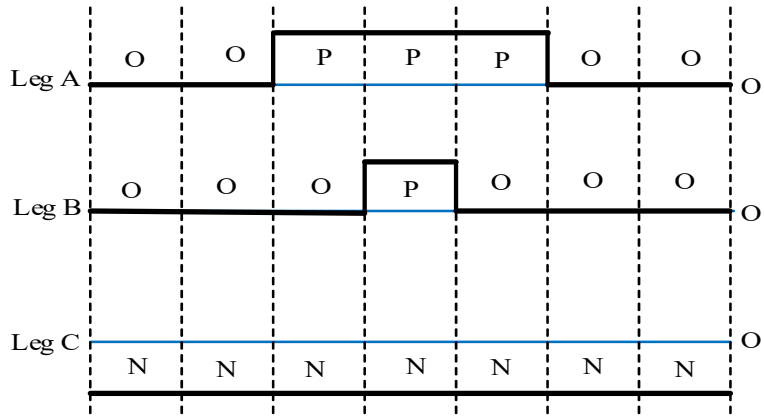
Switching states	Status of switching devices (x=a, b, c) (1=ON, 0=OFF)				Output voltage
	S_{x1}	S_{x2}	S_{x3}	S_{x4}	V_{xo}
P	1	0	0	0	V_{dc1}
O	0	1	1	0	0
N	0	0	0	1	$-V_{dc2}$

4.5.2 Simulation Results

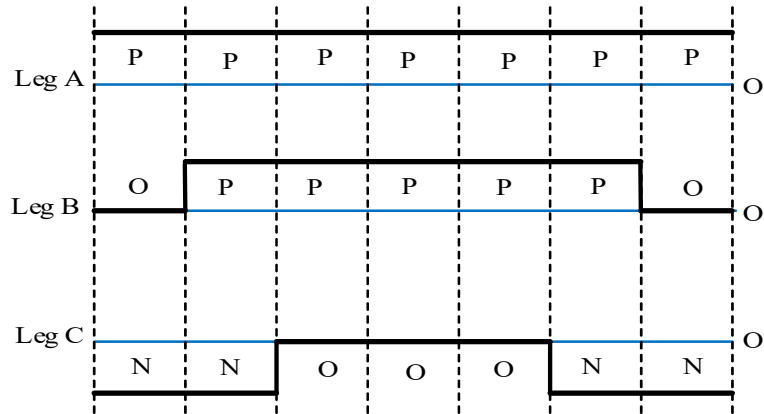
A case study is simulated in PSIM 10 software environment to verify the feasibility and effectiveness of the proposed SVM algorithm with the three-level T-type inverter. The parameters for simulation and experimental implementations of the case study are shown in Table 4.2. It is assumed that there is a detection of thermal overheating in switch S_{a1} in leg A of the inverter (OHF_Flag=1) at time of 0.045 seconds.



(a)



(b)



(c)

Fig. 4.5. Available switching sequences set S in region R4 in the first sextant: (a) S_1 , (b) S_2 , and (c) S_3 .

The performance of the proposed algorithm is compared with the previously addressed approaches in Fig. 4.6. The methodology proposed in [56], which relies on limiting the maximum output current of the inverter, is shown in Fig. 4.6(a). The inverter is driven by normal SVM algorithm until OHF_Flag equals to 1. Then, the reference output current of the inverter is reduced so as to provide relief to the thermally overheated IGBT device. The output voltages remain the same in this approach. Fig. 4.6(b) shows the approach presented in [82], which relies on reducing the modulation index of the inverter and operating with reduced number of output levels in region R1 of each sextant. After detection of the overheating fault (OHF_Flag=1), the voltage of phase A is connected to neutral point O and the modulation index is reduced to operate the inverter in region R1 of the space vector diagram. This approach can effectively reduce the power losses through the device to be zero. However, the output power is dramatically reduced in addition to the increased THD in the output currents.

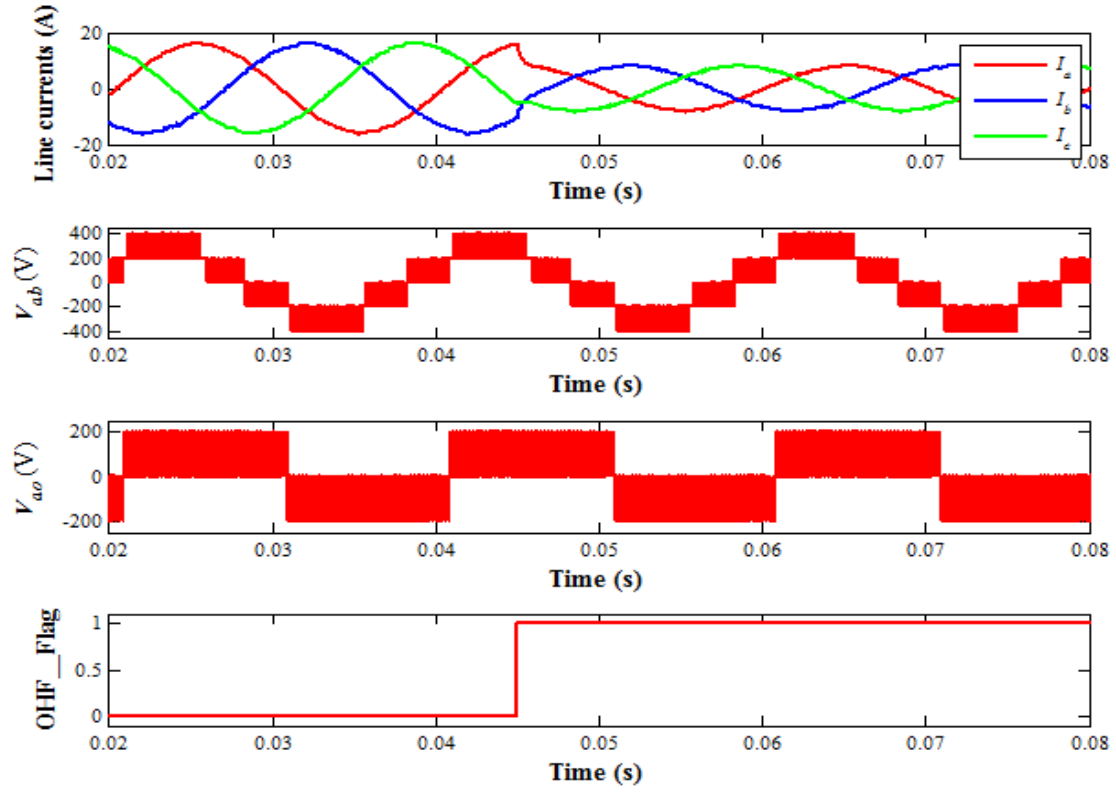
The performance of the proposed algorithm is shown in Fig. 4.6(c). The proposed algorithm preserves the same output currents as in normal SVM. In addition, the proposed algorithm maintains the inverter to continue its operation with the same number of levels in the line voltages as in normal SVM mode. It is clear that the pole voltage V_{an} of the phase leg A, which contains the affected switch, has a different switching pattern than that of normal SVM so as to optimize the power losses through the thermally-aged switch S_{a1} . Compared with other approaches, it is clear that the proposed algorithm is beneficial to prolong the lifetime of the thermally-aged devices without derating of the output currents and the number of the output voltage levels as well.

Fig. 4.7(a)-(c) compare the power losses of power IGBT devices under normal SVM and the proposed SVM algorithm in leg A, leg B, and leg C, respectively. The proposed algorithm introduces a significant reduction in the power losses in the affected IGBT device S_{a1} . As a result, thermal stresses are relieved from the affected device and redistributed to the other less stressed IGBT device S_{a2} under the proposed algorithm. In addition, the power losses of IGBT devices in leg B and leg C of the inverter have not increased at the overheating condition. Fig. 4.7(d) shows the power losses in the thermally-aged device S_{a1} at different modulation indices under normal SVM and the proposed SVM algorithm. It is clear that a significant reduction of the power losses in the affected device is introduced under the proposed SVM algorithm compared to normal SVM.

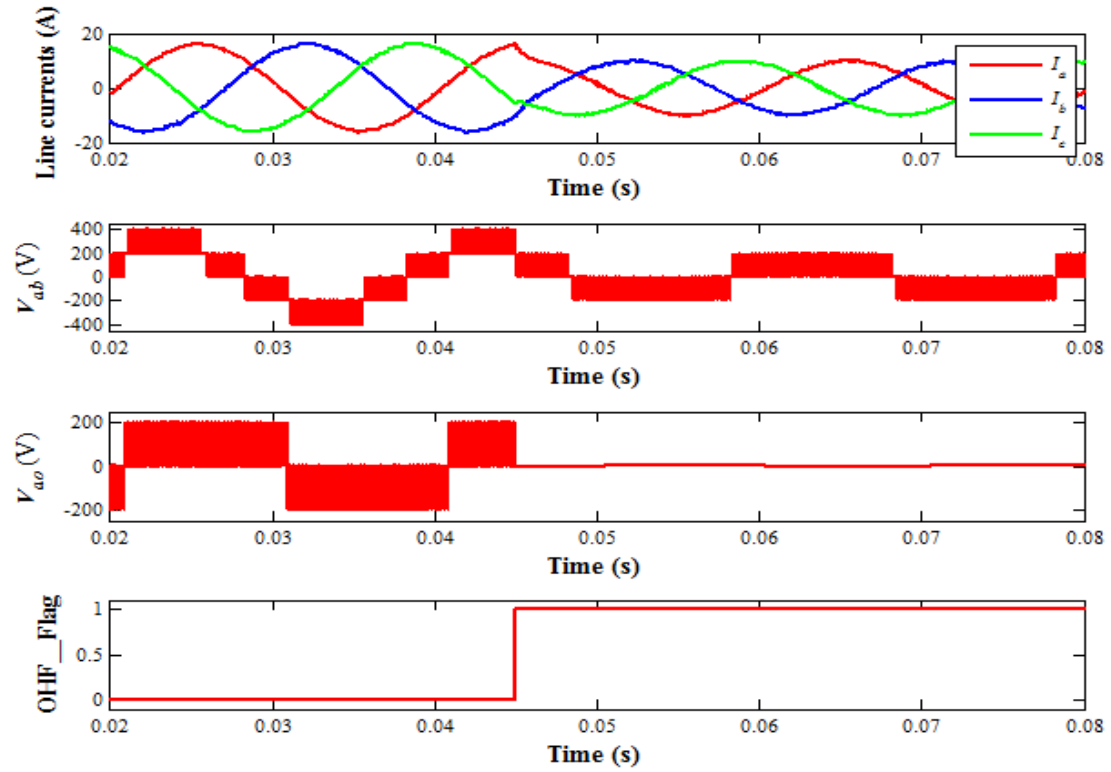
Table 4-2

Parameters of the simulation and experimental study

DC-link voltage V_{dc}	400 V
DC-link capacitance C_1, C_2	1500 μ F
Output frequency f_l	50 Hz
Switching frequency f_s	5 kHz
Modulation index	0.8
Output load resistance R	10 Ω
Output load inductance L	3 mH
Ambient temperature T_a	25°C
Total thermal resistance of IGBT from junction to ambient $R_{th(j-a)}$	4.18°C/W



(a)



(b)

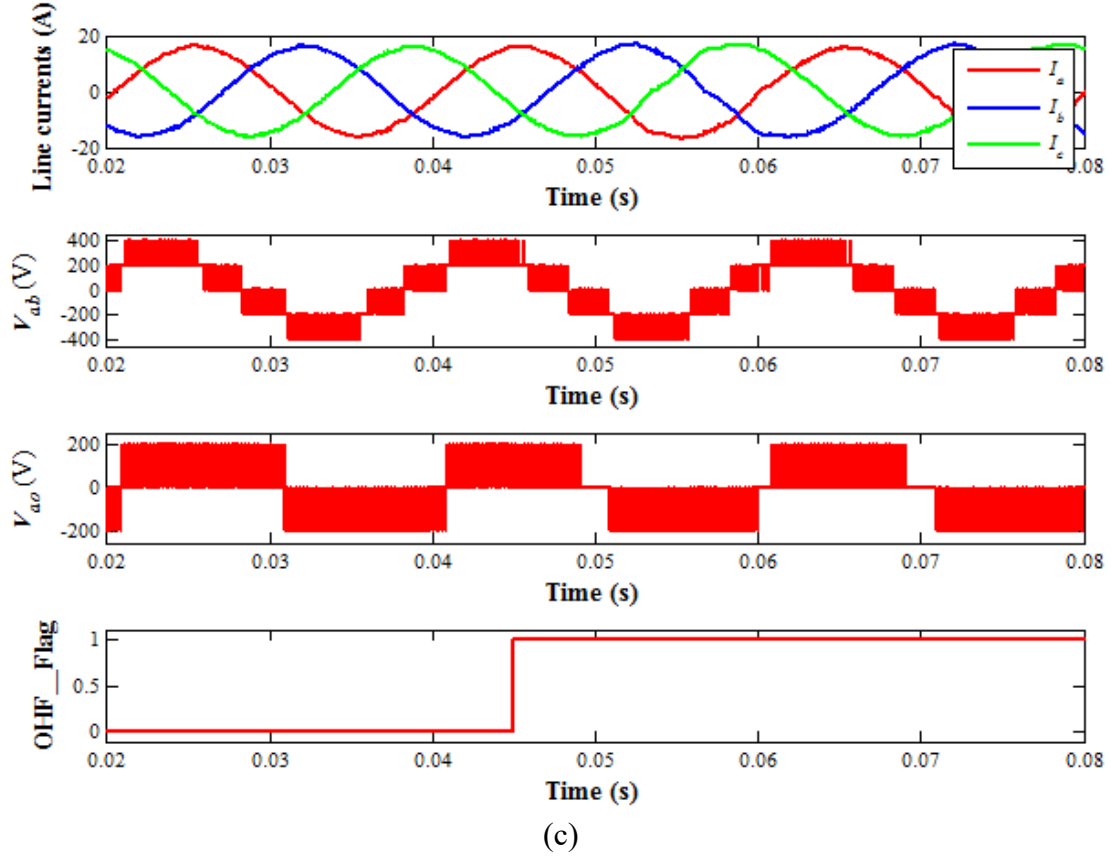
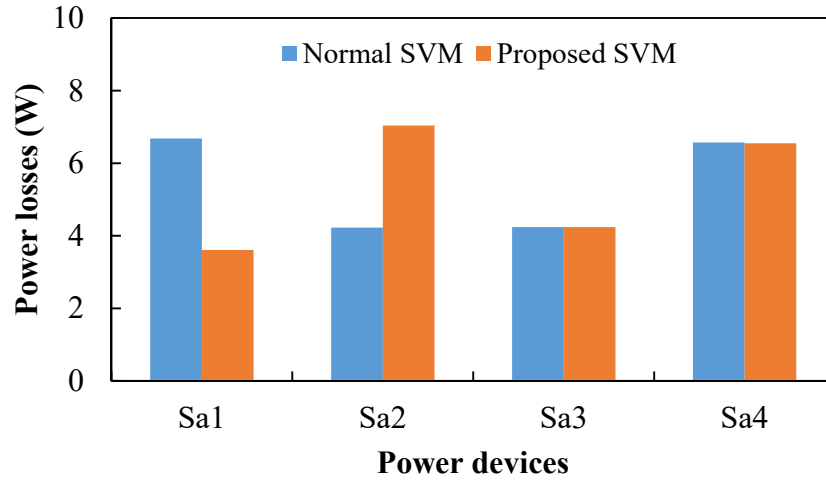
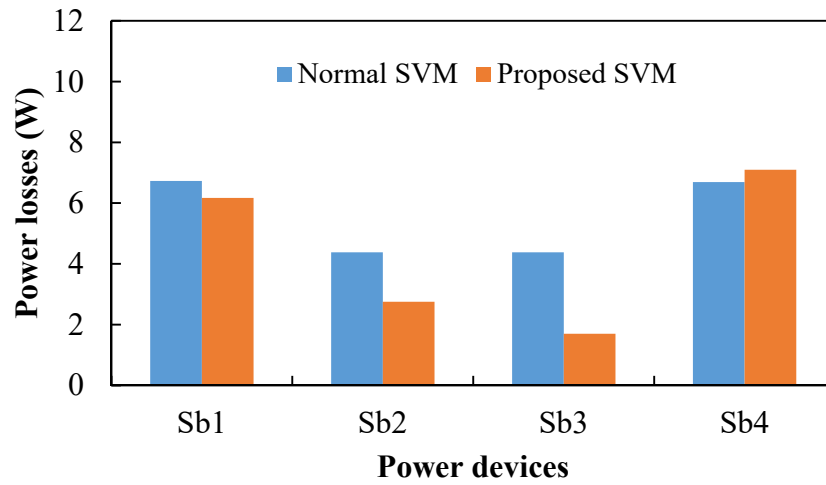


Fig. 4.6. Simulation results of the behavior of lifetime prolongation algorithms: (a) Output current limitation approach. (b) Output levels reduction approach. (c) The proposed algorithm.

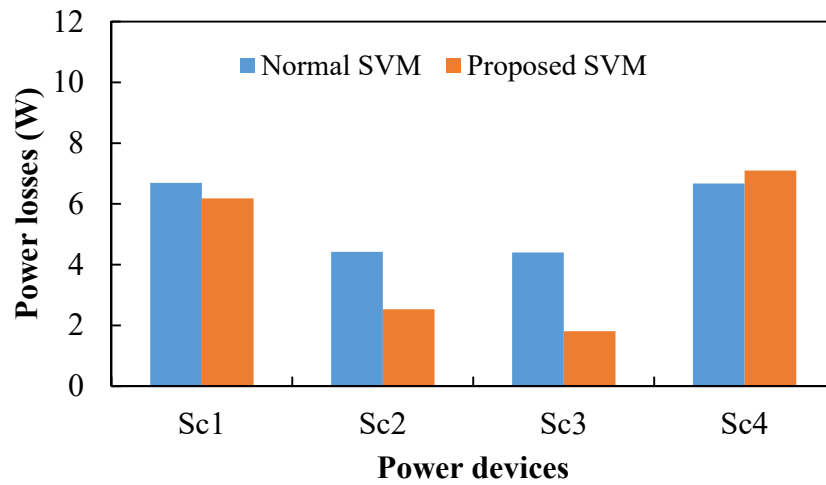
The lifetime of power semiconductor devices is mainly affected by their junction temperature and their temperature fluctuation [47]. Fig. 4.8 compares the junction temperature of the thermally-aged IGBT switch under normal SVM algorithm and the proposed SVM algorithm at different modulation indices. It is clear that the proposed algorithm provides a lower junction temperature than normal SVM algorithm for the whole modulation indices range. This is can be interpreted as a direct benefit of the ability of the proposed algorithm to reduce effectively the power losses through the affected IGBT device S_{a1} . As a result, lifetime prolongation of the thermally-aged device is efficiently performed using the proposed algorithm.



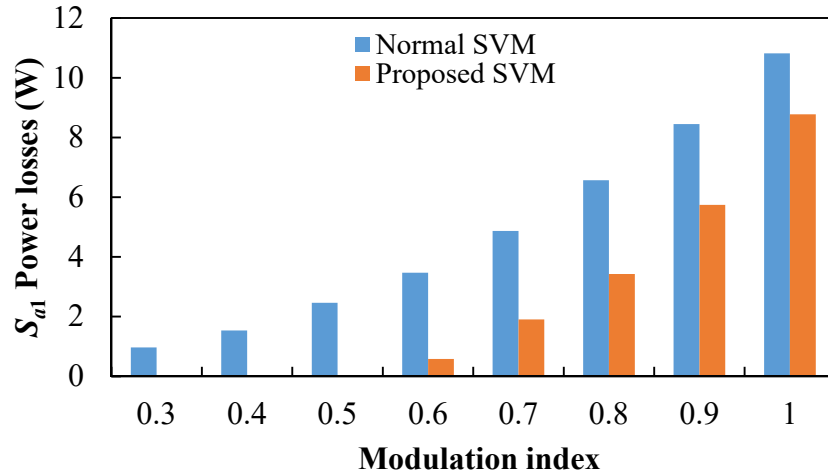
(a)



(b)



(c)



(d)

Fig. 4.7. Comparison of switches power losses under normal SVM and the proposed SVM algorithm at (a)-(c) Semiconductor devices of leg A, leg B, and leg C, respectively at modulation index 0.8, and (d) Thermally-aged device S_{a1} at different modulation indices.

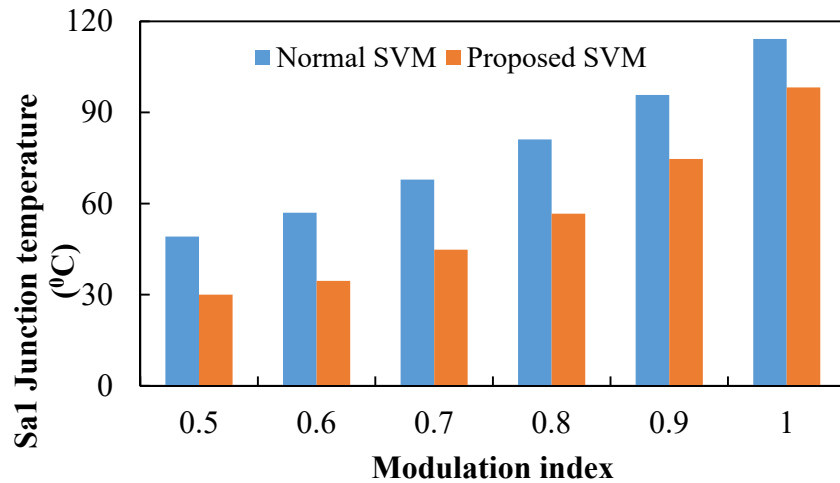


Fig. 4.8. The estimated junction temperature of the thermally-aged device S_{a1} under normal SVM and the proposed SVM algorithm at different modulation indices.

On the other side, a slight increase in the THD of the output currents is introduced under the proposed algorithm compared with normal SVM. Fig. 4.9 compares THD of the output currents under the proposed algorithm and normal SVM algorithm at various modulation

indices. The difference in THD of output currents under the two algorithms is slightly small for the whole modulation indices range. The normal SVM has THD of 3.06% in the output currents, whereas the proposed algorithm has THD of 3.33% at a modulation index of 0.8 for the selected case study.

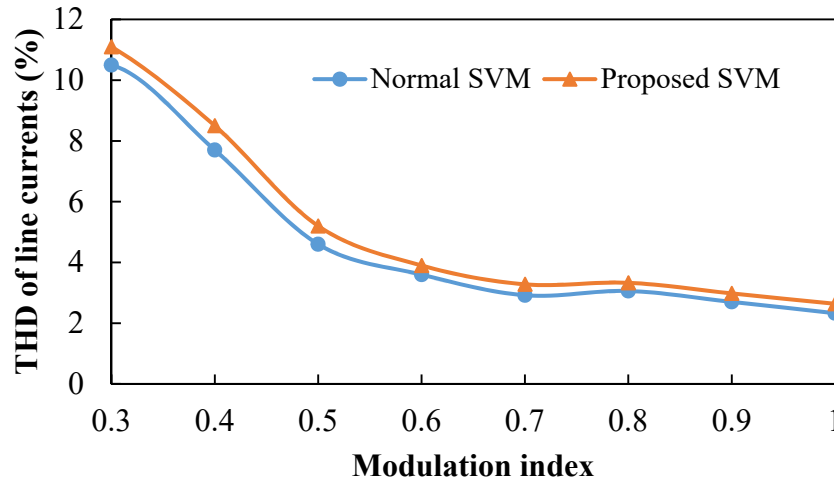


Fig. 4.9. Comparison of THD in the inverter output currents under normal SVM and the proposed SVM algorithm at different modulation indices.

4.6 Experimental Verification

4.6.1 Experimental Results

The proposed algorithm is implemented and verified by an experimental prototype of the three-phase three-level T-type inverter with the same parameters of simulation case study that are shown in Table 4.2. Fig. 4.10 shows the structure of the experimental prototype setup. The control algorithm is implemented on a floating point digital signal processing unit (TMS320F28335). To cope with simulation case study, the test case study of experimental results proposes an overheating has been detected in S_{a1} IGBT in leg A. The thermal aging condition is fed as a digital input for the implemented SVM algorithm.

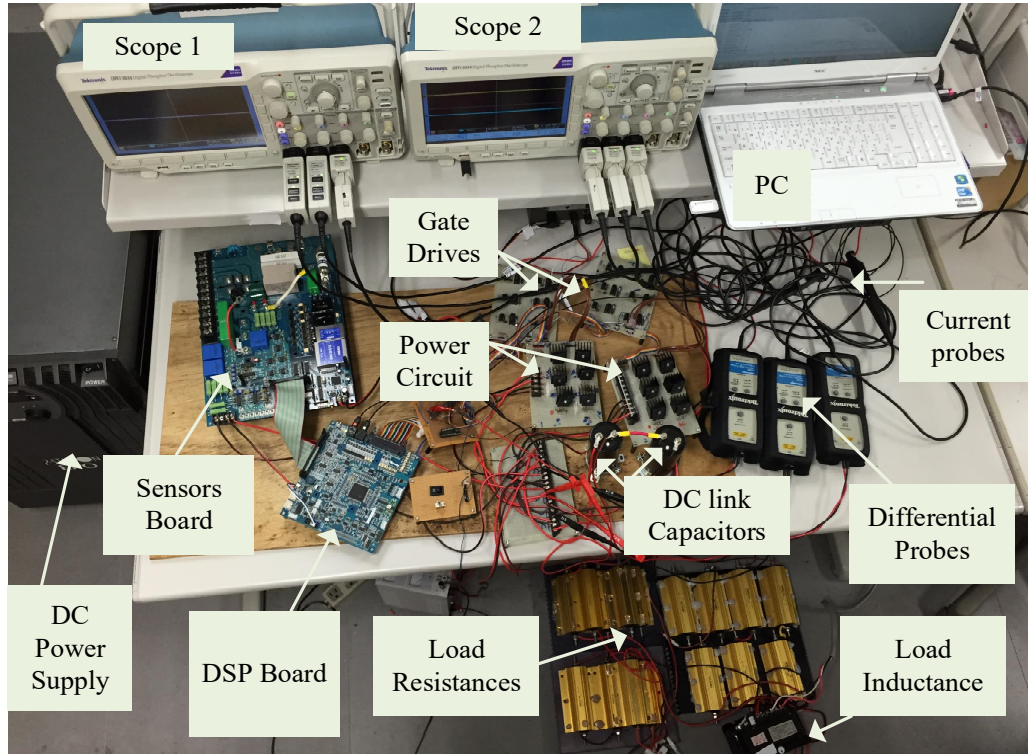


Fig. 4.10. Prototype setup of the three-phase three-level T-type inverter.

The feasibility of the proposed algorithm is verified by comparing its performance with the previously addressed approach in [56]. The performance of the current reduction approach is shown in Fig. 4.11. The line voltage V_{ab} and the pole voltage V_{ao} remain with the same number of levels after OHF_Flag is detected, as shown in Fig. 4.11(a). However, derating of the output currents is required to prolong the lifetime of the thermally aged devices, as shown in Fig. 4.11(b). This approach is suitable for drive applications wherein motors can be driven at derated operation. In addition, this approach can be applied to grid-connected systems as it maintains the same output voltages and the same number of output levels. However, in renewable energy applications, this approach cannot achieve maximum power point tracking (MPPT), which is a key element for economic benefits of this systems.

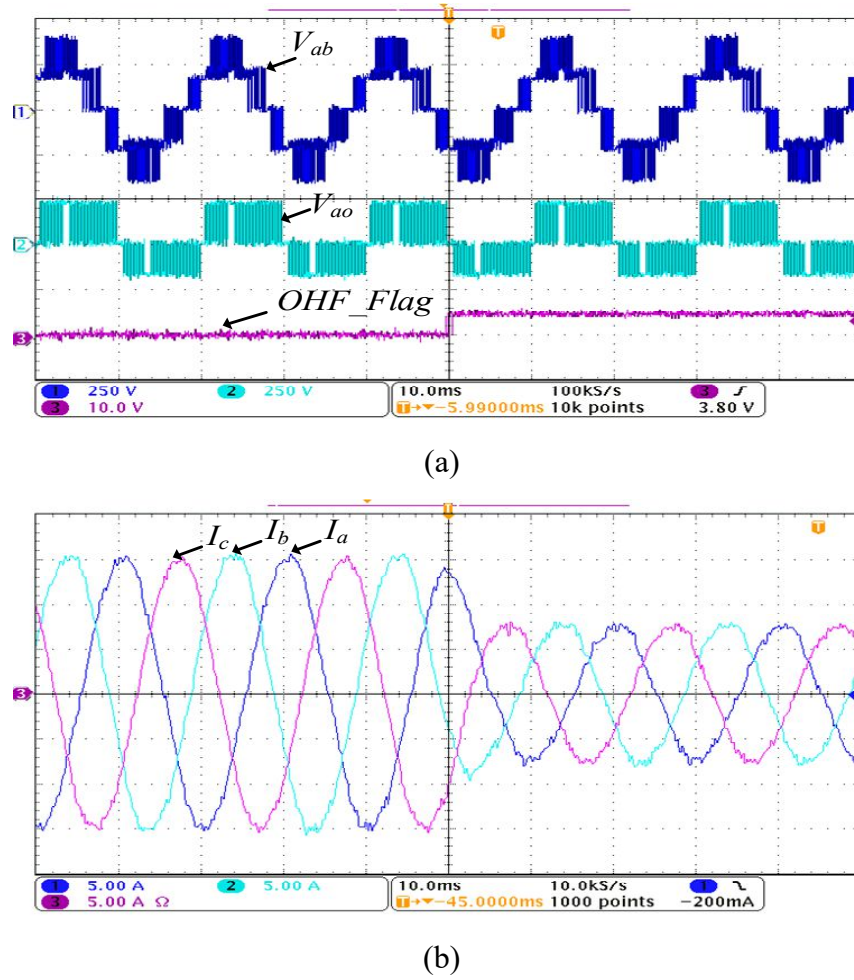
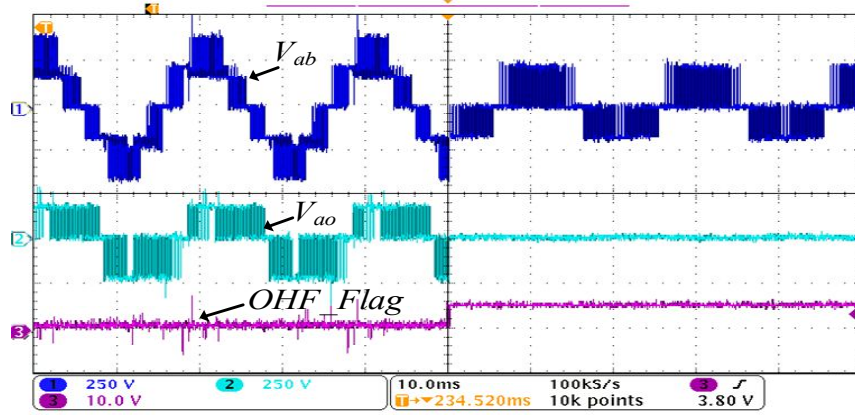


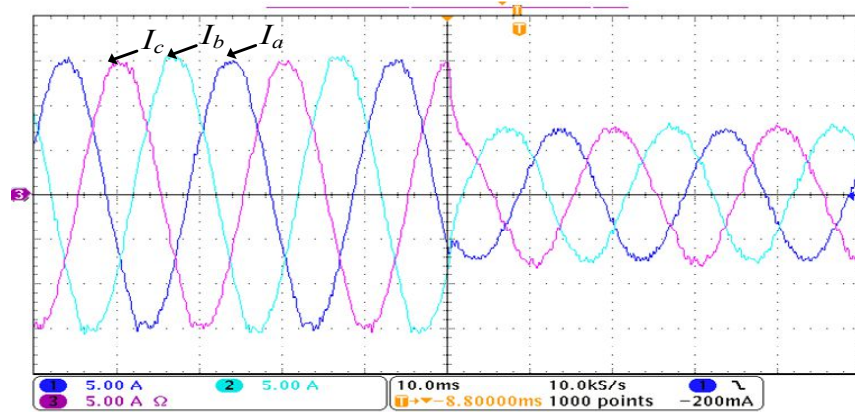
Fig. 4.11. Experimental results of the behavior of the output current limitation approach:
 (a) Line and pole voltages, and (b) Three-phase line currents.

The performance of the output levels reduction approach is shown in Fig. 4.12. The number of levels of the line voltages V_{ab} are reduced, as shown in Fig. 4.12(a) and the pole voltage V_{ao} of leg A is attached to the neutral point O. The modulation index is reduced to be below 0.5 to operate the inverter in region R1 of the sextants of the space vector diagram. Therefore, the output currents are reduced, as shown in Fig. 4.12(b). This method is effective as the faulty leg is held at the NP with no switching or conduction through S_{a1} . The main applications of this method are electrical drive applications and standalone distributed generation systems. However, this method is not suitable for grid-connected

applications due to the reduction of output voltages in addition to the increased THD in their output currents. Moreover, this method is not suitable for MPPT in renewable energy applications.



(a)



(b)

Fig. 4.12. Experimental results of the behavior of the output levels reduction approach:

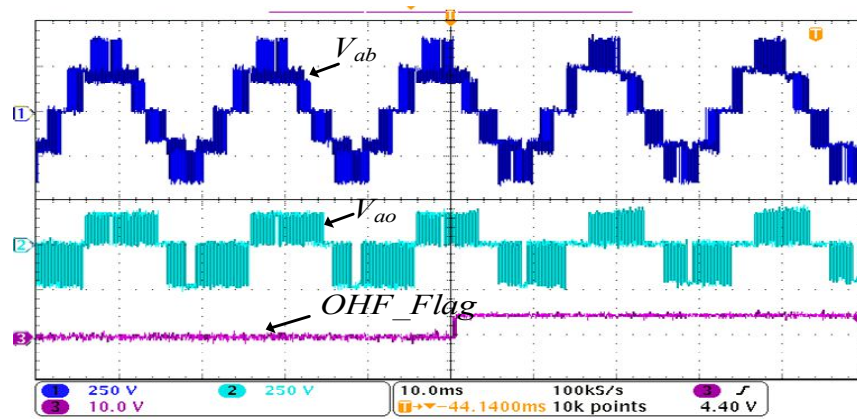
(a) Line and pole voltages, and (b) Three-phase line currents.

Fig. 4.13 shows the experimental behavior of the proposed SVM algorithm. It is clear from Fig. 4.13(a) that the proposed algorithm preserves the same line voltage V_{ab} as in normal SVM. However, the switching patterns of the pole voltage of phase leg A V_{ao} under the proposed algorithm are different from normal SVM. This is due to the operation of the proposed algorithm to relieve the thermally-aged IGBT device S_{a1} using the redundancy

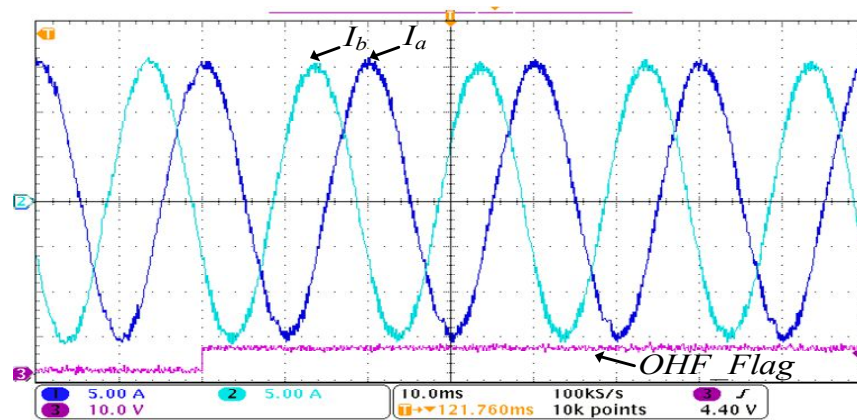
between space vectors. Fig. 4.13(b) shows the performance of the three phase output currents before and after the OHF condition. The output currents remain the same without derating. Therefore, the proposed algorithm is feasible in several applications, including both of electrical drive applications and renewable energy applications with MPPT extraction. Moreover, the proposed algorithm can be applied to stand-alone or grid-connected applications as it preserves the same line voltages without reducing the modulation indices.

Fig. 4.13(c) shows the voltages of DC-link capacitors V_{dc1} and V_{dc2} under normal SVM and the proposed SVM algorithm. The proposed algorithm maintains voltages balance of the DC-link capacitors with introducing a slight increase in the ripples of DC-link voltages. This can be interpreted as the proposed algorithm optimizes the switching sequences so as to provide relief to the thermally-aged IGBT device in regions of space vector diagram that utilize the thermally-aged device. However, the proposed algorithm balances the DC-link voltages in other regions of space vector diagram that do not influence the stresses of the thermally-aged IGBT device. This in accordance verifies the ability of the proposed algorithm to manage different objectives including lifetime prolongation of the devices and voltage balance of DC-link capacitors.

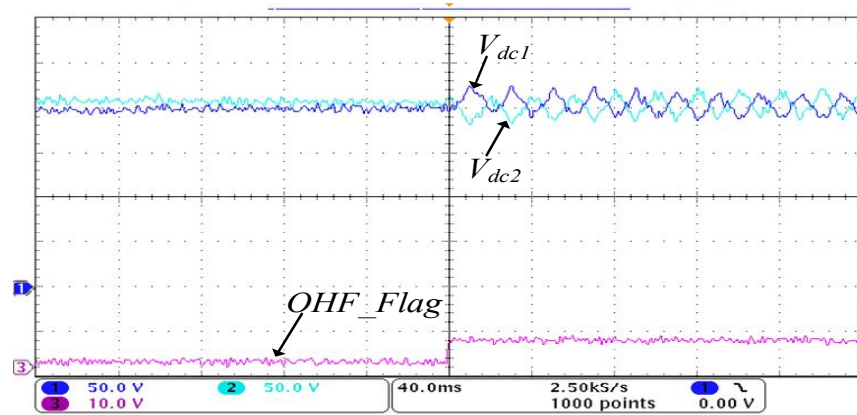
Moreover, the proposed algorithm introduces a little increase in the THD of the output currents of the inverter under the proposed algorithm compared to normal SVM algorithm. The THDs in line currents have been measured experimentally for the selected case study. Normal SVM algorithm has THD in output currents of 3.04% compared to 3.27% in the proposed SVM algorithm.



(a)



(b)



(c)

Fig. 4.13. Experimental results of the behavior of the proposed lifetime prolongation SVM approach: (a) Line and pole voltages. (b) Three-phase line currents and (c) DC-link capacitors voltages.

4.6.2 Comparison with Previous Approaches

Table 4.3 shows comprehensive comparisons of the proposed SVM algorithm with the previously addressed approaches for lifetime prolongation of thermally-aged IGBT devices. Most crucial factors for comparing lifetime prolongation approaches are their requirements of derating the converter's output currents and/or voltage levels and/or using additional components. In addition, the generality of the approach can be recognized by its ability to be applied to an n -level inverter with single and/or parallel operation. Another important factor in this comparison is the effect of applying the approach to the system performances, including the voltages balance of DC-link capacitors, their added voltages' ripples, and THD components in their output currents. The effectiveness of these approaches can be measured by their ability to reduce the power losses through the thermally-aged device. One of the main advantages of the proposed algorithm is its generality. In addition, the proposed algorithm preserves the voltage balance of the DC-link capacitors with a slight increase in their ripples as verified by simulation and experimental results.

4.7 Conclusion

This chapter proposes a novel SVM algorithm to prolong the lifetime of thermally-aged semiconductor devices in multilevel inverters. The proposed SVM method selects the optimal switching sequence that relieves the thermally-aged semiconductor device by using a continual search inside all valid sequences in the current location of the reference vector. The proposed algorithm is generalized that can prolong any of power semiconductor device of n -level inverters independent of the number of output levels. Compared with the previously addressed methods, the proposed SVM method significantly

alleviates the thermal stresses of the thermally-aged devices, while it maintains the same output currents, the same number of output voltage levels, and balanced voltages over DC-link capacitors. The superiority of the proposed algorithm over various lifetime extension techniques has been validated by simulation and experimental results of the three-phase three-level T-type inverter. By similar ways, the proposed methodology can be extended to other types of multilevel inverters. Finally, the proposed method is applied to power IGBT switches and it can be easily applied to other types of power semiconductor devices.

Table 4-3

Comparison of the proposed algorithm with the previously addressed approaches in the literature

Techniques	Performance								
	Current derating	Output levels reduction	Additional component	Application single/parallel/ n -level	DC-link voltages		THD	Effectiveness	Implementation
					Balance	ripple			
TEC device [57]	No	No	-TEC Device -TEC Power - T_j Sensing	Any	Yes	Same	Same	High	Complex
Current reduction [56]	Yes	No	T_j Sensing	Single	Yes	Same	Increase	High	Simple
Level reduction [82]	Yes	Yes	T_j Sensing	Single	Yes	Increase	Increase	High	Moderate
Parallel and interleaved inverters [47]	Yes	No	- T_j Sensing -Full-scale inverters	parallel	Yes	Same	Same	Moderate	Complex
DSVM [64]	No	No	No	Any	Yes	Increase	Increase	Low	Simple
Loss redistribution SVM [59]	No	No	No	3-level	Yes	Same	Slightly increase	Low	Moderate
Ref. [66]	No	No	T_j Sensing	3-level	No	Increase	Increase	Moderate	Simple
Thermal management SVM [65]	No	No	T_j Sensing	Any	Yes	Increase	Increase	Low	Complex
Proposed	No	No	T_j Sensing	Any	Yes	Increase	Slightly increase	High	Moderate

Chapter 5

Conclusions and Future Work

5.1 Conclusions

Out of this search, some important conclusions can be summarized as follows:

1. A new more practical approach for assessment of thermal behavior, and lifetime of RECSs in microgrid operation has been presented. The WECSs with DSTATCOM functionality are selected as a case study for the proposed approach with considering the various modes of resilient operation of microgrids. The main features of the proposed reliability assessment approach are as follows:
 - a. The proposed approach provides a novel methodology for lifetime consumption assessment for multilevel inverters in WECS with DSTATCOM functionality that combines the stochastic behaviors of both wind power and load demands. Compared to the previously addressed reliability assessment methods, this is the first time such joint stochastic behaviors are considered.
 - b. The proposed approach provides a new assessment approach of the thermal stresses and reliability issues of power converters in WECS with the added functionality considering different operating modes of resilient microgrids.
 - c. The proposed approach provides a generalized methodology that considers different topological, configurational, and functionalities changes of WECS and various requirements of systems with WECS integration, which is

considered one of the main salient characteristics featured by the proposed approach.

- d. In addition, the proposed approach provides a straightforward environment for planning and control engineers, in accordance to these evaluations, in order to properly select suitable power components, revalue the added functionalities, and develop new control methodologies.
2. A new method for reliability enhancement of single phase grid connected power inverters has been proposed. The proposed method is based on new pulse width modulation method that extend the operating lifetime of power inverters through achieving thermal stresses relief of the most stressed power semiconductor devices. The proposed method has been verified by results of simulation and experimental prototypes. A generalized implementation of the proposed method, to provide thermal stresses relief for any of the components and for any n-level inverters, is also presented. Compared to the existing thermal management methods, the proposed strategy can offer the following merits.
- a. The proposed reliability enhancement method retains the same benefits as the conventional carrier PWM methods, i.e., a simple and easy implementation,
 - b. The proposed method provides a significantly reduced power losses and thermal stresses of the stressed semiconductor devices through adaptively selecting the redundant switching states in each switching cycle, in order to optimize power losses through the thermally-stressed device. Moreover, the proposed method enhance the reliability in twofold through reducing both of

the junction temperature and temperature cycling of the stressed device compared with normal mode operation of the device.

- c. Moreover, the proposed strategy maintains the inverter operation with the same output ratings, and voltage balance over DC-link capacitors.
3. A novel method to enhance the reliability of grid connected three-phase renewable energy generation systems has been proposed through developing new space vector modulation (SVM) method that relieves the thermally-aged semiconductor device by using a continual search inside all valid sequences in the current location of the reference vector. The superiority of the proposed algorithm over various lifetime extension techniques has been validated by simulation and experimental results of the three-phase three-level T-type inverter. Compared to the previously addressed methods, the proposed method features the following advantages:
- a. One of the main advantages of the proposed algorithm is its generality. The proposed algorithm can prolong any of power semiconductor device of n -level inverters independent of the number of output levels. By similar ways, the proposed methodology can be extended to other types of multilevel inverters. Moreover, the proposed method is applied to power IGBT switches and it can be easily applied to other types of power semiconductor devices.
 - b. Compared with the previously addressed methods, the proposed SVM method significantly alleviates the thermal stresses of the thermally-aged devices, while it maintains the same output currents, the same number of output voltage levels, and balanced voltages over DC-link capacitors.

5.2 Future Work

1. Extending the reliability assessment and enhancement of power converters in RECSs to develop new reliability aware power converters and controllers.
2. Integrate the proposed methods of reliability assessment and enhancement in RECSs design and component selection for reliability.
3. Investigating more comprehensive condition monitoring method that considers the developed estimation method of reliability.
4. Extending the reliability enhancement through investigating new fault tolerant topologies that can compensate for the total damage of power devices in single and three phase RECSs.

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