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Performance and Stability Analysis of Negative Capacitor in OLED Driving Circuit

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Abstract: We have demonstrated in the previous work that the negative capacitor can effectively prevent the signal delay due to the parasitic capacitance in the current programmed OLED display. However, there were some problems in the real panel application. Therefore, we discussed the difference between the simulation and measurement results and proposed the methods to improve the negative capacitor performance. We also analyzed the stability of negative capacitor considering the parasitic resistance as well as the capacitance. Especially in the case of large display where the data line has large parasitic resistance, the negative capacitance value should be smaller than that of parasitic capacitance or the delay components should be inserted in negative capacitor for stability.

Keywords: OLED, Current program, Negative capacitor, Parasitic capacitance, Stability

1. Introduction

In these days, organic light-emitting diode (OLED) is started to appear in mobile electronics, car electronics, and TVs. Compared with liquid crystal display (LCD), it has many advantages such as high brightness, wide viewing angle, good color gamut, high response time, etc. While LCD uses a constant voltage to drive the system, a constant current is needed to drive both of the passive-matrix (PM) and the active-matrix (AM) driven OLEDs to avoid the degradation of organic materials and the non-uniformity of brightness. In the current-programmed AMOLED, the driving transistor in each pixel is used as a current source and the data signal should be supplied to the gate of the driving transistor in selecting period. But, the variation of transistor properties between pixels causes serious image quality degradation called 'mura', and many researches have been reported in several ways such as voltage programming method[1)-3)], current programming method or digital driving method[4)-6)]. Among them, the current programming method is considered to be the best method in terms of the image quality and the production yield, because it can compensate both threshold voltage (V_{th}) and field effect mobility variations while the voltage programming method can compensate only the variation of V_{th}, and the digital driving method has difficulties in the fine resolution display. However, the current programming method has a serious problem on the delay of current setting time, because the small current supplied from the data driver cannot charge up the huge parasitic capacitance of the data-bus-line within a selecting period. In PMOLED that uses a constant current to drive OLED, this signal delay problem also occurs because the unselected OLED pixels behave as a large parasitic capacitance. Several attempts have been tried so far to solve this problem such as pre-charging method, voltage or current feedback method[7)-10)]. But, there are many problems in these methods: difficulties of precise control, a margin of error related to the measurement of voltage or current, and too big space to be in an IC chip.

We have obtained very significant results on this problem in the previous work using a new concept called 'negative capacitor', which has the same quantity as parasitic capacitance but has negative sign[11)-13)]. The negative capacitor, which is composed with a differentiation circuit, an inverting amplifier and a voltage-to-current converter as shown in **Fig.1**, can easily be adjusted to the various kinds of panels and can be simply designed inside the driving IC chip. According to the simulation results with the ideal device model, the data signals in the small current level such as 10 nA could be settled within a short period such as 10 μsec[11)]. In the real PMOLED panel composed with lumped elements in a breadboard, the negative capacitor could express a quite excellent gradation in image even in the low current level comparing with the circuit without that[12)]. However, contrary to the simulation results, the signal delay in the testing panel was as large as 16 μsec at the minimum current level. Although the large parasitic capacitance of PMOLED panel (2.3 nF) was considered, the reason why the function was degraded in the low current level could not be explained thoroughly. In this paper we will deal with the origin of

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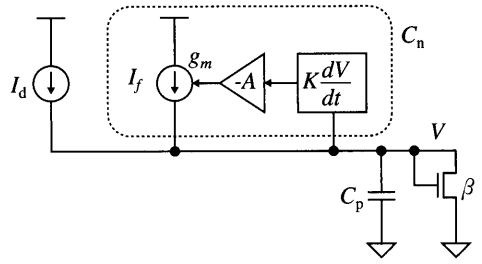

Fig.1 Conceptual circuit diagram of negative capacitance circuit surrounded with a dotted line and simplified current-programmed AMOLED pixel circuit.

the difference between simulation and real panel results, and we are going to propose the design method for negative capacitor.

Another unclear point on the application of negative capacitor will be the circuit stability. Although the result of the small PMOLED panel application might verify the stability, enough investigation should be considered for large TV target. We have already considered the possibility of negative capacitor circuit for large TV application[13]. According to this, there is no difference of signal delay between far and near side pixel, but it seems that the instability increases in the far side pixel. One of the biggest differences between small and large displays is that there are parasitic resistances on the data lines in the latter case. We will discuss in this paper the effect of the data line parasitic resistance on the circuit stability, and also deal with the design method of stable negative capacitor circuit.

2. Design Method for Negative Capacitor

The negative capacitor is composed of a differentiation circuit, an inverting amplifier, and a voltage to current converter as shown in **Fig.1**. Among them, the voltage to current (V/I) converter can be considered as the most important component to its properties. Generally, the simplest form of V/I converter that can realize linear property is composed of an OP-AMP with a negative feedback loop, a MOS transistor, and a resistor as shown in **Fig.2**[14]. The output current is proportional to $(V_{DD}-V_{in})/R$ in this circuit. This simple V/I converter is not so widely used in the IC design because the variation of resistor is quite large in LSI. However, we can use it in our negative capacitor free from the concern of the spatial variation or temperature fluctuation because, in our negative capacitor circuit, the value of negative capacitance can be presented with the ratio of resistances which are used in the differentiation circuit, the inverting AMP, and the V/I converter.

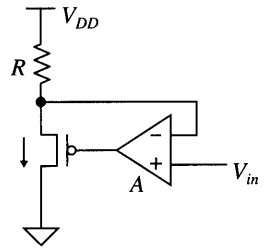

Fig.2 Voltage to current converter circuit.

Two methods to control the current coming from the V/I converter can be considered: one is the method that has the DC bias current in V/I converter like **Fig.3 (a)** and the other is the method that has no DC bias current like **Fig.3 (b)**. Therefore, the application

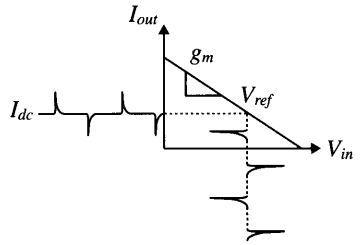

Fig.3 (a) Transconductance curve of V/I converter with DC current.

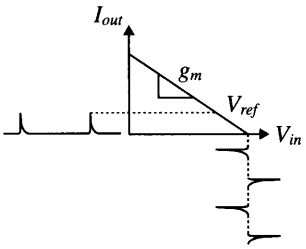

Fig.3 (b) Transconductance curve of V/I converter without DC current.

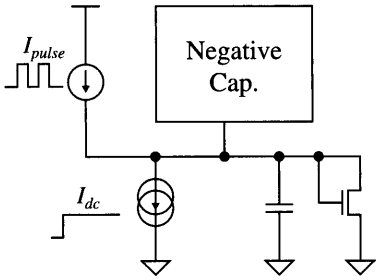

Fig.3 (c) Circuit diagram of PIDS (Pulse Input-DC sink).

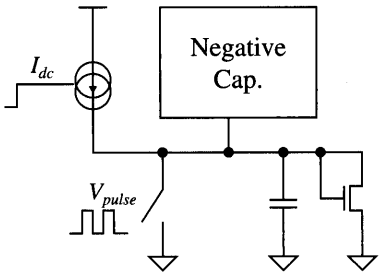

Fig.3 (d) Circuit diagram of DIPS (DC Input-Pulse Sink).

method of negative capacitor leads two different ways. If there is DC bias current in V/I converter, we need to add the DC current sink component to remove it, and we call this system Pulse Input DC Sink (PIDS). On the other hand, in the case of no DC current bias, we don't need the DC current sink component but the pulse off component to make the current pulse. In this case, the V/I converter cannot produce the negative differentiation signal, and we call this system DC Input Pulse Sink (DIPS). In PIDS method, the same quantity of DC current as that from the V/I converter should be removed by the DC sink, if not, the pixel current signal may be distorted. But, it is not easy to realize the precisely controlled bias current source in the IC. Therefore, DIPS method is desirable for practical use.

Figure 4 shows the pixel currents simulated by SPECTRE from CADENCE Co. The pulse signal with 120 μsec width and 200 μsec period was delivered to the PMOLED pixel whose parasitic capacitance was assumed to be 2.3 nF. When we changed the gain of the OP-AMP used in the negative capacitor, more distorted signal was acquired in the case of the lower OP-AMP gain. These phenomena are more severe in the low current level. From these results, it seems that the difference between the simulation and the real panel measurement results in our previous works[11),12)] comes from the difference between ideal OP-AMP with an infinite gain and real OP-AMP with a finite gain. The property of V/I converter that shows the threshold characteristics in the transconductance curve as shown in **Fig.5** can explain these phenomena. While the large voltage variation from the reference voltage can make some current flow, the small voltage variation less than the threshold voltage cannot make any current flow in I_{out}. This phenomenon has originated from the structure of V/I converter in **Fig.2**. In the beginning, the positive and negative input terminals of OP-AMP have the same potential. When the voltage change is inputted to the positive terminal, the voltage change, whose value is the product of voltage difference between two terminals and finite gain of OP-AMP, is acquired in the output terminal of OP-AMP. When this output voltage is applied to the MOS gate, no current will flow through the MOS if the voltage difference between the source and the gate is not larger than the threshold voltage of MOS. Therefore, V/I converter will not operate until the input voltage is above a certain value.

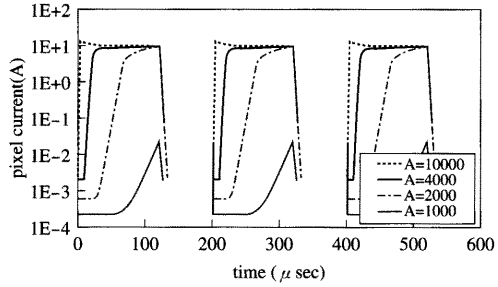

Fig.4 Simulated pixel currents of PMOLED with various OP-AMP gain in the negative capacitor. The period of input signal is 200 μsec, the width is 120 μsec, and the maximum value is 10 μA.

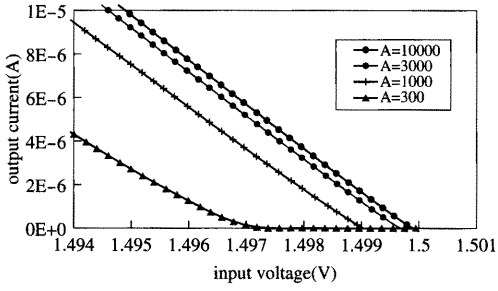

Fig.5 Simulated transconductance curve of V/I converter with various OP-AMP gain.

To relieve this threshold characteristics in the V/I converter, three methods can be considered: lowering the V_{th} of MOS, getting a large OP-AMP gain, or controlling OP-AMP's off-set voltage to cancel out the threshold voltage. Although we can lower the threshold voltage of V/I converter using these 3 methods, it seems not so easy to realize that. However, because we don't have to get a perfect device, we may design only to satisfy the requested specification. There is a reference voltage (V_{ref}) in the transconductance curve as shown in **Fig.6**, and the current starts to be generated from the point of V_{ref}-V_{th}. While the slope of the curve is proportional to the inverse of resistance, when the voltage is V_{min}, which is the minimum voltage in the normal operation range of V/I converter, the current flow reaches the maximum value, which is determined by the size of MOS and the bias voltage of OP-AMP. That is, as the width of MOS is larger or the V_{SS} of OP AMP is lower, V_{min} gets lower. The relation between V_{min} and V_{th} can be determined by the following equation, so that the ratio of maximum and minimum pixel currents can be accommodated in the linear range in **Fig.6**,

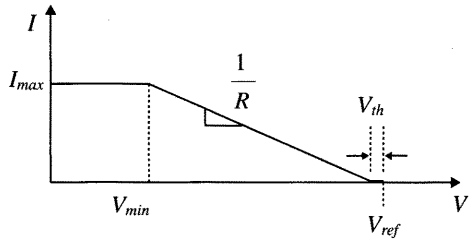

Fig.6 Transconductance curve of V/I converter.

$$\frac{V_{ref}-V_{\min}}{V_{ref}-V_{th}} > \frac{I_{\max}}{I_{\min}} \tag{1}$$

where I_{max} and I_{min} are the maximum and minimum values of pixel current specification.

3. Stability Analysis

In the case that no resistance is assumed in data lines, the stable condition is given as $C_n < C_p$. In case of $C_n \geq C_p$, the system gets unstable and diverges. Therefore, the condition where C_n is slightly smaller than C_p is the best to obtain the stable and shortest current programming time. However, there is some parasitic resistance on bus-line in real panel circuit, and for simple calculation we divided it into 2 categories as shown in **Fig.7**: far side pixel and near side pixel.

3.1 For the near side pixels

The relation between the current and voltages of the near side pixel which is located near the driver IC as shown in **Fig.7 (a)** can be obtained by the following equations:

$$i_{in} = g_m (v - v_0) - C_n \frac{dv}{dt} + C_p \frac{dv_e}{dt} \tag{2}$$

$$v = R_p \left\{ C_p \frac{dv_e}{dt} \right\} + v_e \tag{3}$$

$$i_{out} = g_m (v - v_0) \tag{4}$$

where, v_e represents the voltage at the node of parasitic capacitor, and v is the voltage at the node of driving transistor. Assuming the small signal conditions, the V-I characteristics of diode-connected transistor was expressed by the linear relation with the transconductance of g_m. Equations (2), (3) and (4) can be transformed to the following equations by Laplace transformation.

$$I_{in} = g_m V - C_n sV + C_p sV_e \tag{5}$$

$$V = R_p C_p sV_e + V_e \tag{6}$$

$$I_{out} = g_m V \tag{7}$$

The transfer function given by the ratio of input and output current is represented by:

$$G(s) = \frac{I_{out}}{I_{in}} = \frac{g_m (R_p C_p s + 1)}{g_m + (g_m R_p C_p - C_n + C_p)s - C_n R_p C_p s^2}. \tag{8}$$

The poles of this transfer function are found as follows:

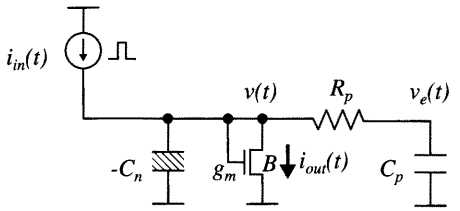

Fig.7 (a) Equivalent circuit of the near side pixel data line.

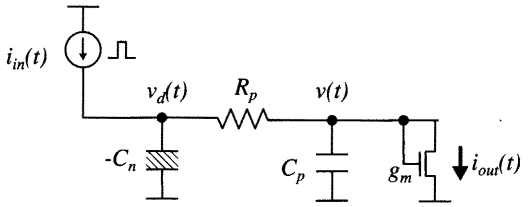

Fig.7 (b) Equivalent circuit of the far side pixel data line.

$$p_{1,2} = \frac{\left[(g_m R_p C_p - C_n + C_p) \pm \sqrt{(g_m R_p C_p - C_n + C_p)^2 + 4 C_n R_p C_p g_m} \right]}{2 C_n R_p C_p}. \tag{9}$$

Both of these poles are located on the real axis in s-plane and the larger pole is always located in the positive side, which means that this system is unstable. Therefore, unfortunately the negative capacitance circuit in the practical panel is not stable as long as the data-line has some resistance.

We can avoid this instability problem by inserting the delay element in the negative capacitance circuit. If the negative capacitance circuit has the delay element with time constant, T, then Eq. (5) is represented by

$$I_{in} = g_m V - C_n \frac{1}{1+Ts} sV + C_p sV_e. \tag{10}$$

This equation gives the transfer function as follows:

$$G(s) = \frac{I_{out}}{I_{in}} = \frac{g_m (R_p C_p s + 1)(1 + Ts)}{\left[(g_m R_p C_p T - R_p C_p C_n + C_p T) s^2 + (g_m R_p C_p + g_m T - C_n + C_p) s + g_m \right]}. \tag{11}$$

The poles of this function are found as follows:

$$p_{1,2} = \frac{\left[-(g_m R_p C_p + g_m T - C_n + C_p) \pm \sqrt{(g_m R_p C_p + g_m T - C_n + C_p)^2 - 4 g_m (g_m R_p C_p T + C_p T - R_p C_p C_n)} \right]}{2 (g_m R_p C_p T + C_p T - R_p C_p C_n)}. \tag{12}$$

The stability condition of poles can be expressed as follows:

Table 1 Stability condition of the circuits with negative capacitor for the far side pixels.

	$C_n < C_p$	$C_n = C_p$	$C_n > C_p$
$T < C_nR_p$	Conditionally stable	Unstable	Unstable
$T = C_nR_p$	Stable	Unstable	Unstable
$T > C_nR_p$	Stable	Stable	Conditionally stable

$$C_n < \left(g_m + \frac{1}{R_p}\right)T. \tag{13}$$

It means that C_n does not depend on the value of C_p in terms of stability, so C_n can be even bigger than C_p as long as T increases. We can also consider the general case: if C_n=C_p and T= C_nR_p, then the transfer function G(s) becomes 1 like Eq. (14).

$$G(s) = \frac{(R_pC_ps+1)(1+C_nR_ps)}{(C_pR_ps+1)^2} = 1. \tag{14}$$

Therefore, it can be said that the system for the near side pixel can be stable only if delay component which satifies Eq. (13) is inserted in the negative capacitor.

3.2 For the far side pixels

The same calculation can be applied to the case of far pixels in **Fig.7 (b)**, and leads to the following equations:

$$i_{in} = -C_n\frac{dv_d}{dt} + C_p\frac{dv}{dt} + g_m(v - v_0) \tag{15}$$

$$v_d = R_p\left\{C_p\frac{dv}{dt} + g_m(v - v_0)\right\} + v \tag{16}$$

$$i_{out} = g_m(v - v_0) \tag{17}$$

where, v_d represents the voltage at the node of negative capacitor, and v is the voltage at the node of driving transistor. The transfer function given by the ratio of input and output current is represented by:

$$G(s) = \frac{I_{out}}{I_{in}} = \frac{g_m}{g_m - C_nC_pR_ps^2 + (C_p - C_n - C_nR_pg_m)s}. \tag{18}$$

The poles of this transfer function are found as follows:

$$p_{1,2} = \frac{\left[C_p - C_n - C_nR_pg_m \pm \sqrt{(C_p - C_n - C_nR_pg_m)^2 + 4C_nC_pR_pg_m}\right]}{2C_nC_pR_p}. \tag{19}$$

Because one of these poles is always located in the positive side in s-plane, this system also can be said to be unstable. So, if we also insert the delay element with time constant, T, in the negative capacitance circuit, then the transfer function becomes the following equation:

$$G(s) = \frac{I_{out}}{I_{in}} = \frac{g_m(1+Ts)}{\left[C_p(T - C_nR_p)s^2 + \left[g_m(T - C_nR_p) - (C_n - C_p)\right]s + g_m\right]}. \tag{20}$$

The poles in this function are found as follows:

$$p_{1,2} = \frac{\left[(C_n - C_p) - g_m(T - C_nR_p) \pm \sqrt{\left[g_m(T - C_nR_p) - (C_n - C_p)\right]^2 - 4g_mC_p(T - C_nR_p)}\right]}{2C_p(T - C_nR_p)} \tag{21}$$

The results of stability conditions, which were determined by the signs of poles, are summarized in **Table 1**, where "stable" means both of the poles are located in the negative side in s-plane, and "unstable" means one of the poles are located in the positive side, and "conditionally stable" means that the stability can be changed by other conditions like g_m. In the case of C_n= C_p and T = C_nR_p, it is hard to judge the stability with poles in s-plane, because both the denominator and the numerator of poles approaches zero. So, when we develop the transfer function of Eq. (20) in this case, we can get the following equation.

$$G(s) = 1 + Ts. \tag{22}$$

This means that the transfer function consists of the first order lead element and the system will sensitive at the frequency higher than 1/T. Therefore, we need to add the delay element to the input signal, that is, to cut off the high frequency in the input signal.

4. Summary

We studied the design method of negative capacitor circuit, and we knew that the V/I converter design was the most important factor. OP-AMP with a finite gain makes the threshold characteristics in the V/I converter, so that the negative capacitor circuit cannot work at the low current level signal. We can solve this problem by lowering the V_{th} of MOS, using an OP-AMP with large gain, or controlling OP-AMP's offset voltage to cancel out the threshold voltage. But, it seems not so easy to realize these methods in the real

applications. However, because we have only to make it to meet the requested user specification, we can use the method of resistance control in the V/I converter or bias voltage control in OP-AMP in accordance with the ratio of maximum and minimum pixel current specification.

The stability of negative capacitor circuit, especially in large display with parasitic resistance, was investigated. To make a simple analysis, we divided the display equivalent circuit into the far and the near side pixels, and we found that the system was not always stable even if negative capacitance was equal to parasitic capacitance. Therefore, the value of negative capacitor should be set smaller than parasitic capacitance or delay elements should be put in the negative capacitor circuit.

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